SPECIAL FEATURE

HPEC System Strategies in Defense

Affordable and Approachable HPEC Technologies Meet New Defense Needs

High-performance embedded computing is a major requirement for the compute-heavy needs of many of today's military systems. But the trick is to achieve an affordable solution that's straightforward to implement.

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When most defense program contractors think of high-performance embedded computing (HPEC) systems, they envision huge behemoth solutions that can take on the most labor-intensive processing that would have taxed lesser computing technology only a few years ago. That perception is definitely accurate with HPEC systems continually advancing to allow command and control units to see or detect smaller objects in a bigger field. Today's cameras have up to a massive 20K plus field of view with amazing resolution from pixel points that go on forever. That camera input requires HPEC systems to process huge amounts of data. And, the latest extremely sensitive sensor-based systems deliver capabilities that leapfrog previously developed technology.

Two Types of HPEC Needs

Available computing architectures have enabled defense program developers to build a very broad spectrum of HPEC applications to match diverse requirements. When developers evaluate computing solutions, they typically have two different types of needs for HPEC. The first is compute-bound, which demands multiple processors to solve a problem, without the need for extensive bandwidth capabilities.

The second type of HPEC system is I/O-bound, where application data comes in and is split or shared between systems that do little work with the data but needs high-bandwidth connectivity between processors and with the outside world. Supporting the high-end camera example previously mentioned is a separate I/O-bound application that would be used to push all this data down to a ground station. That requires enough bandwidth to enable the system to parse the data out for access by varying systems and personnel, enabling them to make intelligent decisions.

There seems to be no end in sight for increasingly advanced defense capabilities that can be achieved from the processing of multi-sensor data. The prevailing development approach for HPEC is to look for specialized silicon primarily adopting FPGAs as the solution that will allow systems to react immediately to data and perform electronic warfare algorithms and co-processing functions.

All that said, the latest with HPEC solutions is that they've been evolving quietly but steadily. They've progressed to where they can be implemented in much smaller standards-based platforms—rather than in the perceived mega-computing solutions currently deployed. Many new HPEC system needs can actually be handled now with more mainstream IT technology packaged in a compact way in a 3U VPX-based system that balances I/O and CPU power with high-speed I/O backplanes and multicore x86 processing architectures.

Why Mainstream IT Makes Sense

Tackling many of the HPEC-type problems that used to require highly sophisticated architecture with mainstream IT solutions is really an advantage for defense contractors. They can save their most experienced engineering resources for complex, large-scale systems that still require that level of expertise. Instead of requiring a lot of specialty hardware, I/O and switch fabric to qualify as an HPEC system, developers now have access to proven technologies such as Intel multicore processors, PCIe and 10/40 Gbit Ethernet, which allows a complete HPEC compute engine to be built off of only standards-based components. For example, Intel architecture provides co-processing capabilities with a GPU that enable designers to include specific-function FFTs for 3D radar applications. This eliminates extra design steps to offload certain functions from an all-standard architecture.

Plus, there is widespread engineering familiarity with mainstream IT technologies such as x86 processors, TCP-IP and the PCIe interface. This means a broader knowledge base can implement HPEC systems from laptops to high-end servers or even a conduction-cooled, ruggedized HPEC for a UAV or ground program. Developers can now tackle larger

Figure 1
VXFabric provides the required software between the PCIe Gen 3 switch and the bottom of the standard TCP/IP stack to enable boards to run any existing TCP/IP-based application without having to be modified.

HPEC requirements that used to require specific proprietary solutions with well-known architectures that are easier to program and deploy. Experienced embedded computing suppliers have application-ready, small COTS VPX-based 3U solutions readily available.

Endless Performance Appetite

The task of meeting mounting data processing needs from defense OEMs that typically request "as much performance as you can give us" is now met with the realities of tightening budgets and the fact that new technology is not created or needed every year. Defense contractors remain competitive by developing new technology templates that can be used for multiple programs and are viable solutions for three to five years. Without huge budgets and unlimited user support, defense contractors are finding it more difficult to support specialized silicon, language and fabric solutions. In addition, technology advancements move too fast to re-imagine new architectures from scratch.

This is where COTS-based computing suppliers come in to help. They have proven building blocks and system solutions with the algorithms required mapped onto the computing architecture. Fewer OEM specialists are needed when HPEC suppliers can meet defense program metrics by delivering the ultra-fast speeds they need on the backplane in a much smaller footprint. It also helps that COTS suppliers have the experience to accommodate new proof-of-concept requirements.

Affordable, Approachable Solutions

Mainstream HPEC building blocks naturally reduce costs and provide an approachable engineering solution due to their standards-based platform methodology. They are proven to support everything from Gbyte/s performance needed for current radar systems, to tens of Gbytes/s needed for camera interfaces, and also satisfy five plus teraflops of computing power required for 3D radar.

Taking HPEC from the data center into the field are simplified standards-based multicore platforms that solve high connectivity and low latency interconnects requirements. This approach gives basic skill level engineers the ability to build effective systems using modular processor interconnect fabrics that implement the TCP/IP protocol over the PCI Express infrastructure. The result is a tenfold increase in I/O performance with no porting effort, well-suited for most HPEC-based applications. Figure 1 shows an example solution along those lines. Experienced suppliers

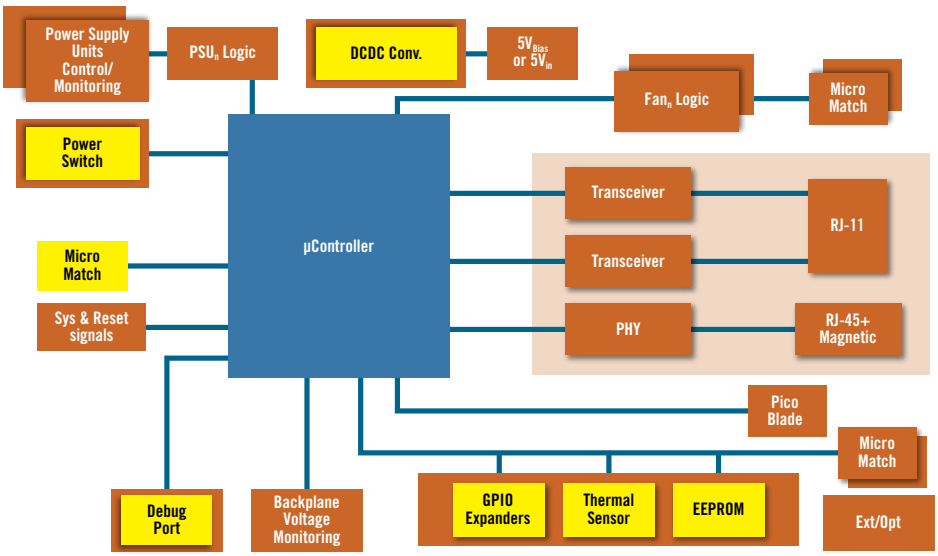

Figure 2
VXControl implements detailed out-of-band health management at the computer level. It enables necessary computer control and management ranging from serial line interface to SNMP networking connections.

that offer mainstream HPEC platforms are able to support customers by building the computing portion of the application or giving them the right tools that streamline the replacement of a significant size system now with a couple of 3U VPX boards housed in a rugged, small chassis.

It also helps that COTS suppliers have the experience to accommodate new proof-of-concept requirements. In any complex application that requires a lot of processing power and I/O, there is the need to do upfront evaluation and benchmarking to ensure the system will meet specifications—from input rates, processing rates to the output.

Tools to Get the Job Done

HPEC isn't just for what developers consider the most compute-intensive applications anymore—HPEC fits a wider spectrum of program needs. But experienced and novice developers, too, still need tools to streamline the design process.

Understanding system health management status is more important than ever with continued technology advancements. A good example is the changing clock speed to match battery demand in x86 processor architectures. While varying clock speed is fine for individual PCs, it isn't good for military embedded systems that depend upon multiple computers and boards where each board has a different clock cycle that can result in an unstable power system. Health management software tools that control speed and computing power in one place are the answer. Available today are 3U VPX box-level systems that integrate a computer management board (CMB) for extensive health status information at the board and sub-rack level. Information such as airflow temperature can be controlled for each slot, and payload boards can be held in standby mode to accommodate low-energy surveillance mode. Figure 2 shows an example of a computer management board (CMB) that does system health management.

Another way these tools are valuable is to ensure more realistic lab testing that simulates the stresses and environmental conditions where a system will be deployed. Simplification is key in testing new ideas, so using mainstream TCP/IP makes it so much easier to go from the lab to deployment with the same technology. Waiting until the last stage of development and integration to find out that the algorithm doesn't perform to mission standards is very unwelcome news. A tool such as this becomes invaluable in terms of designing for power management when one considers that a typical user's guide for today's chipset devotes 12 pages to defining power management guidelines.

Ready Mainstream HPEC Solutions

Approaching the problem of HPEC with complexity is no longer necessary. Current 3U VPX systems strike the right balance between CPU computing power and I/O bandwidth by leveraging high-speed switched PCIe and 10 Gbit Etherneton the backplane. These VPX-based, multiprocessor and highly integrated HPEC systems meet defense program performance and bandwidth specifications, making it far less attractive to use more proprietary architectures.

Furthermore, these modular pre-integrated HPEC solutions ensure longevity and flexibility while also providing beneficial customization features, enabling system designers to meet specific requirements of multiple programs. The modular building block approach makes way for future system upgrades, eliminating the need for a complete system redesign.

Figure 3
StarVX is based on a 3U VPX platform architecture, and provides up to 6 Gbytes/s sustained bandwidth on the data plane through TCP/IP and 4 Gbytes/s on the PCIe backplane from a high-speed switch fabric, VXFabric.

The use of standard communication protocols such as TCP/IP or UDP/IP allows OEMs to protect their application software investments. Developers can design legacy software to operate in the current application, and if the requirements evolve or change, new software based on TCP/IP is ensured to be supported for years to come. This design approach enables OEMs to optimize the total cost of ownership (TCO) and have a direct migration path from their existing application to systems deployed in the future. Figure 3 shows an embedded HPEC solution using TCP/IP over PCI Express.

Untapped Potential

There is certainly untapped potential for defense OEMs to implement mainstream HPEC platforms that have reached a milestone using VPX to satisfy size, weight and power (SWaP) demands while at the same time delivering the higher performance and bandwidth. Because major jumps in technology occur in cycles, incremental program improvements and not just the toughest computing problems, offer new revenue streams for HPEC. These upgrades or mid-range systems can benefit from smaller machines that can get the job done.

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