» User Guide «

CP690HS

Active PMC Carrier Board
for CompactPCI Applications

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July 16, 2009

Revision History

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Table of Contents

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List of Tables

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List of Figures

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Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.

Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.

Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.

Note ...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

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Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

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Special Handling and Unpacking Instructions

ESD Sensitive Device!

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Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

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In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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Chapter 1

Introduction

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1. Introduction

1.1 Overview

PMC modules are renowned for their flexibility and versatility of use. They afford the user wide-ranging system-independent solutions by means of easily interchanged or upgraded mezzanine add-on modules. The CP690HS has been designed to maximize the advantages provided by PMC modules in a 6U environment. Flexibility, versatility, convenience and ease of use have been keynotes throughout the design process. The result is a board which, although essentially a carrier for PMC modules, also includes a wide range of important features such as a PCI-to-PCI bridge, rear I/O capability, and the ability to hot swap. Use of the hot swap feature means, of course, that all PMC modules employed on the board are effectively hot-swappable.

The CP690HS is a 6U non-intelligent, active CompactPCI carrier board with two single-size PMC slots.

Some of the outstanding features of the CP690HS are:

- Active carrier with PCI-to-PCI bridge
- 32/64-bit, 33/66 MHz PCI bus on the CompactPCI (primary) and on the PMC (secondary) side with the following configurations:
  - 32-bit/33 MHz CompactPCI bus with 32-bit and 33 MHz PMC bus
  - 64-bit/66 MHz CompactPCI bus with 32/64-bit and 33/66 MHz PMC bus
- It supports the interrupts INTA, INTB, INTC, and INTD
- Software transparence: a specific software driver is required for using the hot swap feature
- It may be configured either for 3.3V or 5V signalling on the secondary PCI bus (PMC side)
- It supports all the signals of the PCI bus on its connectors Jn1 (J11/J21), Jn2 (J12/J22) and Jn3 (J13/J23)
- The two Jn4 connectors J14 and J24 provide the possibility to implement rear I/O through the CompactPCI connectors J3 and J5.
- The connectors which connect the mezzanine board with the carrier include all the signals of a 66/33 MHz, 64/32-bit, multi-master PCI bus, the power rails for 3.3V, 5V, +12V, -12V, V(I/O) and other specialized signals for board detection.
- A PCI-to-PCI bridge provides for coupling of the PMC side to the CompactPCI side, so that two independent PCI busses exist. The PCI-to-PCI bridge is the Pericom PI7C8154B. It is software transparent and consequently a software driver is not required to manage data transfer between the PMC module and the CompactPCI bus.
- The CP690HS has been designed to function with all Kontron CompactPCI backplanes. The fact that the J4 connector is not present on the CP690HS means that this carrier board can also be used in systems employing an H110 backplane.

Kontron's PMC modules are operable in both CompactPCI and VME systems. They offer all the key benefits of PC I/O technology, namely:

- Low-cost solutions
- High performance
- A processor-independent local I/O bus
- A broad range of I/O peripheral devices

Customers who additionally require the functionality of the CP690HS in the smaller 3U form factor are referred to Kontron's single-height PMC Module carrier board, the CP390.

1.2 Optional Modules

1.2.1 CP-RIO6-90 Dual PIM Rear I/O Transition Module

The CP-RIO6-90 rear I/O transition module has been designed for use only with the CP690HS 6U CompactPCI board from Kontron and enables the user to connect up to two PIM modules to the CP690HS.

For further information on this rear I/O transition module, refer to Appendix A, “CP-RIO6-90”.

1.3 System Relevant Information

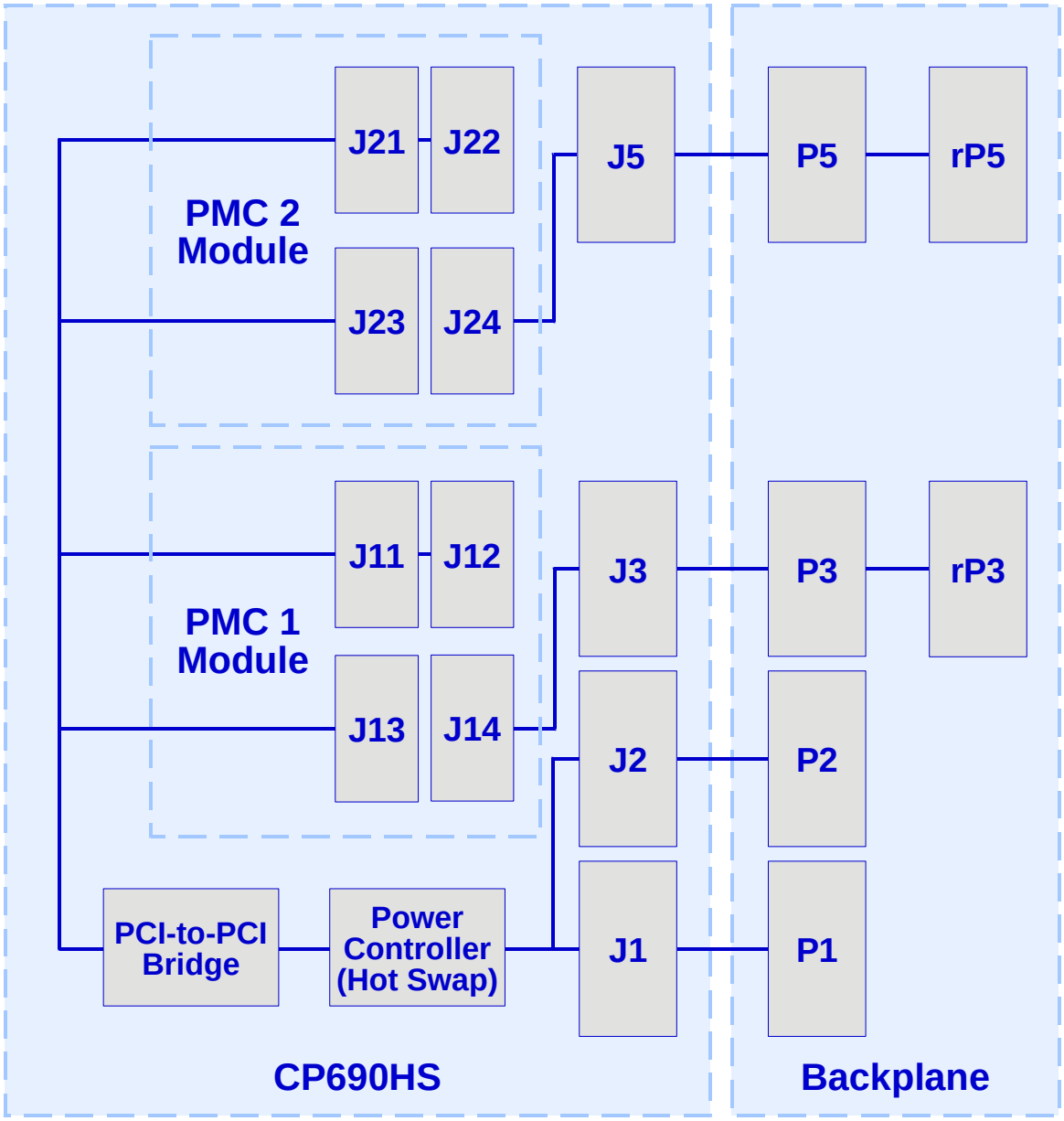
The following system relevant information is general in nature but should still be considered when developing applications using the CP690HS.

Table 1-1: System Relevant Information

SUBJECT	INFORMATION
Master/Slave Functionality	The CP690HS can operate only as a slave board.
Board Location in the System	The CP690HS board must be installed in a peripheral slot of a CompactPCI backplane.
Hot Swap Compatibility	The CP690HS is hot swap capable in compliance with the PICMG 2.1 R1.0 Hot Swap specification.
Hardware Requirements	The CP690HS can be installed in any CompactPCI 6U rack.

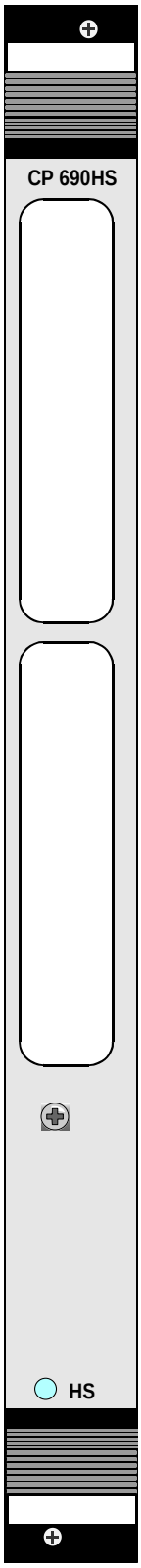
1.4 Functional Block Diagram

Figure 1-1: Functional Block Diagram



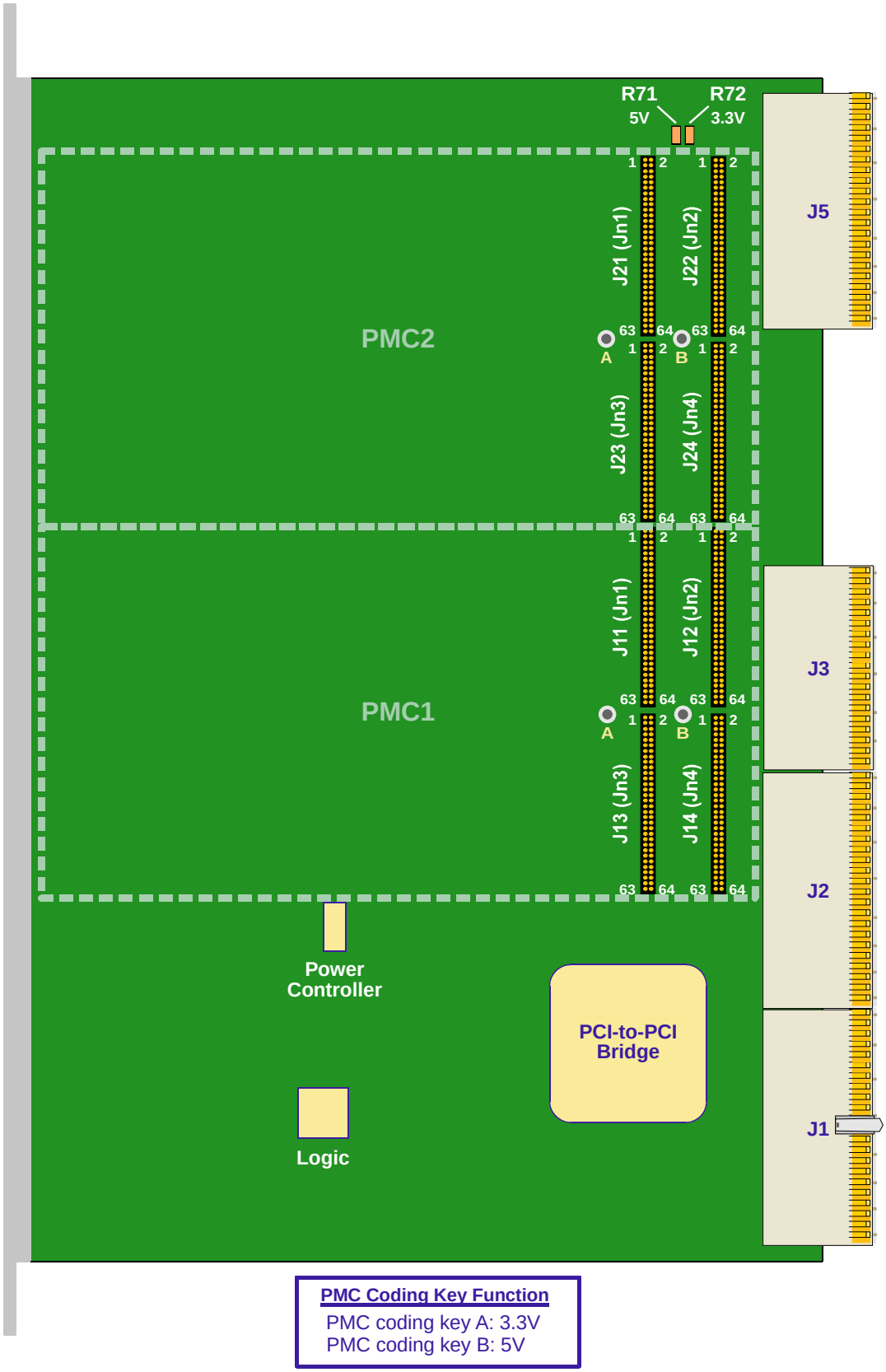
1.5 Front Panel

Figure 1-2: Front Panel



1.6 Board Layout

Figure 1-3: Board Layout



1.7 Technical Specifications

Table 1-2: CP690HS Main Specifications

CP690HS		SPECIFICATIONS
Interfaces	PCI-to-PCI Bridge	• Pericom PI7C8154B P2P bridge controller
	CompactPCI	Compliant with CompactPCI Specification PICMG® 2.0 R 2.1 • Peripheral operation • 32/64-bit at 33/66 MHz master interface • Universal signaling support The desired CompactPCI bus speed must be stated on the order.
	Rear I/O	• PMC rear I/O
	Hot Swap Compatible	The CP690HS is hot swap capable in compliance with the PICMG 2.1 R1.0 Hot Swap specification.
	PMC	CMC / PMC P1386 / Draft 2.4a compliant mezzanine interface • Jn1, Jn2, Jn3 and Jn4 PCI mezzanine connectors for standard single-size PMC modules • 64/32-bit, 66/33 MHz PCI interface • User-selectable configuration to 3.3 V or 5 V (default configuration 3.3 V) • Rear I/O supported through the CompactPCI connectors J3 and J5
Sockets	Front Panel	• Two PMC front panels
	Onboard Connectors	• PMC interface (connectors Jn1, Jn2, Jn3, and Jn4) • CompactPCI connectors J1, J2, J3, and J5
General	Mechanical	6U, 4HP, CompactPCI-compliant form factor
	Power Consumption	max. 3.9 W See Chapter 6 for further details.
	Temperature Range	Operational: 0°C to 60°C Standard -25°C to 75°C E1 Storage: -55°C to 85°C
	Climatic Humidity	93% RH at 40 °C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	233.35 mm x 160 mm
	Board Weight	275 g
HW Monitoring	LED	System status: • HS (blue): Hot swap control

1.8 Standards

This product complies with the requirements of the following standards:

Table 1-3: Standards

COMPLIANCE	TYPE	STANDARD	TEST LEVEL
CE	Emission	EN55022 EN61000-6-3	--
	Immission	EN55024 EN61000-6-2	--
	Electrical Safety	EN60950	--
Mechanical	Mechanical Dimensions	IEEE 1101.10	--
Environmental and Health Aspects	Vibration (Sinusoidal)	IEC60068-2-6	10-300 [Hz] 2 [g] 1 [oct/min] 10 cycles/axis 3 axes
	Shock	IEC60068-2-27	30 [g] 9 [ms] 3 shocks per direction 6 directions 5 [s] recovery time
	Bump	IEC60068-2-29	15 [g] 11 [ms] 500 bumps per direction 6 directions 1 [s] recovery time
	Vibration, broad-band random (digital control) and guidance	IEC 60068-2-64	20-500Hz, 0.05[g²] 500-2000Hz, 0.005[g²] 3.5 [g RMS] 30 [min] test time/axis 3 axes
	Climatic Humidity	IEC60068-2-78	93% RH at 40 °C, non-condensing
	WEEE	Directive 2002/96/EC	Waste electrical and electronic equipment
	RoHS	Directive 2002/95/EC	Restriction of the use of certain hazardous substances in electrical and electronic equipment

1.9 Related Publications

The following publications contain information relating to this product.

Table 1-4: Related Publications

PRODUCT	PUBLICATION
CompactPCI Systems and Boards	CompactPCI Specification 2.0, Rev. 3.0 CompactPCI Hot Swap Specification PICMG 2.1 Rev. 1.0 Draft Standard for a Common Mezzanine Card Family, P1386/Draft 2.0 Draft Standard Physical and Environment Layers for PCI Mezzanine Cards, P1386.1/Draft 2.0
PMC/PIM	PMC I/O Module Standard VITA 36 - 199X, Draft 0.1, July 19, 1999

Chapter 2

Functional Description

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2. Functional Description

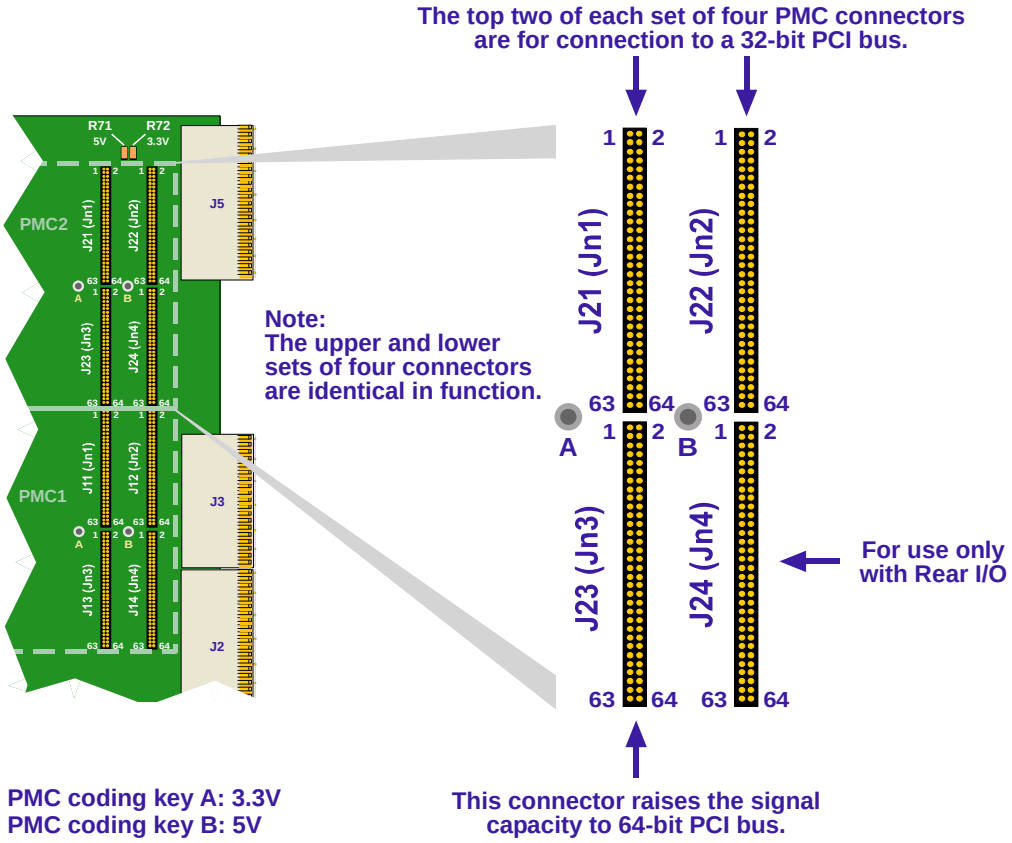
2.1 Board Interfaces

2.1.1 PMC Slots

The two single-size PMC slots on the CP690HS provide an easy way to extend a CompactPCI system via the wide array of interfaces and functions which are available from all PMC vendors. The secondary (PMC) side of the PCI-to-PCI bridge provides a 32/64-bit wide PCI data path with a speed of up to 66 MHz which is routed to the onboard connectors Jn1, Jn2 and Jn3. These connectors also provide the power supply for the PMC module. The PMC slots have been designed to comply with the IEEE 1386.1 specification, which defines a PCI electrical interface for the CMC (Common Mezzanine Card) form factor.

The CP690HS has been designed to comply with the CompactPCI hot swap specification PICMG 2.1 R1.0, which means that the power supply of the PMC modules will be ramped up and a reset generated whenever the board is plugged into a running system. The CP690HS provides 3.3V (default) and 5V PMC PCI signaling environment.

Figure 2-1: PMC Connectors Functions



Warning!

The PMC coding key must be set according to the chosen PMC voltage.

Care must be taken to ensure correct voltage configuration. Using an incorrect signalling voltage may damage the PMC module.

2.1.1.1 PMC Connectors Pinout

Table 2-1: PMC1 and PMC2 Connectors Jn1 and Jn2 Pinouts

Jn1 (J11/J21)				Jn2 (J12/J22)			
SIGNAL	PIN	PIN	SIGNAL	SIGNAL	PIN	PIN	SIGNAL
TCK	1	2	-12V	+12V	1	2	TRST#
Ground	3	4	INTA#	TMS	3	4	TDO
INTB#	5	6	INTC#	TDI	5	6	Ground
BUSMODE1#	7	8	+5V	Ground	7	8	PCI-RSVD*
INTD#	9	10	PCI-RSVD*	PCI-RSVD*	9	10	PCI-RSVD*
Ground	11	12	PCI-RSVD*	BUSMODE2#	11	12	+3.3V
CLK	13	14	Ground	RST#	13	14	BUSMODE3#
Ground	15	16	GNT#	3.3V	15	16	BUSMODE4#
REQ#	17	18	+5V	PCI-RSVD*	17	18	Ground
V(I/O)	19	20	AD[31]	AD[30]	19	20	AD[29]
AD[28]	21	22	AD[27]	Ground	21	22	AD[26]
AD[25]	23	24	Ground	AD[24]	23	24	+3.3V
Ground	25	26	C/BE[3]#	IDSEL	25	26	AD[23]
AD[22]	27	28	AD[21]	+3.3V	27	28	AD[20]
AD[19]	29	30	+5V	AD[18]	29	30	Ground
V(I/O)	31	32	AD[17]	AD[16]	31	32	C/BE[2]#
FRAME#	33	34	Ground	Ground	33	34	PMC-RSVD
Ground	35	36	IRDY#	TRDY#	35	36	+3.3V
DEVSEL#	37	38	+5V	Ground	37	38	STOP#
Ground	39	40	LOCK#	PERR#	39	40	Ground
SDONE#	41	42	SBO#	+3.3V	41	42	SERR#
PAR	43	44	Ground	C/BE[1]#	43	44	Ground
V(I/O)	45	46	AD[15]	AD[14]	45	46	AD[13]
AD[12]	47	48	AD[11]	M66EN	47	48	AD[10]
AD[09]	49	50	+5V	AD[08]	49	50	+3.3V
Ground	51	52	C/BE[0]#	AD[07]	51	52	PMC-RSVD
AD[06]	53	54	AD[05]	+3.3V	53	54	PMC-RSVD
AD[04]	55	56	Ground	PMC-RSVD	55	56	Ground
V(I/O)	57	58	AD[03]	PMC-RSVD	57	58	PMC-RSVD
AD[02]	59	60	AD[01]	Ground	59	60	PMC-RSVD
AD[00]	61	62	+5V	ACK64#	61	62	+3.3V
Ground	63	64	REQ64#	Ground	63	64	PMC-RSVD

Table 2-2: PMC1 and PMC2 Connector Jn3 Pinout

Jn3 (J13/J23)			
SIGNAL	PIN	PIN	SIGNAL
PCI-RSVD	1	2	Ground
Ground	3	4	C/BE[7]#
C/BE[6]#	5	6	C/BE[5]#
C/BE[4]#	7	8	Ground
V(I/O)	9	10	PAR64
AD[63]	11	12	AD[62]
AD[61]	13	14	Ground
Ground	15	16	AD[60]
AD[59]	17	18	AD[58]
AD[57]	19	20	Ground
V(I/O)	21	22	AD[56]
AD[55]	23	24	AD[54]
AD[53]	25	26	Ground
Ground	27	28	AD[52]
AD[51]	29	30	AD[50]
AD[49]	31	32	Ground
Ground	33	34	AD[48]
AD[47]	35	36	AD[46]
AD[45]	37	38	Ground
V(I/O)	39	40	AD[44]
AD[43]	41	42	AD[42]
AD[41]	43	44	Ground
Ground	45	46	AD[40]
AD[39]	47	48	AD[38]
AD[37]	49	50	Ground
Ground	51	52	AD[36]
AD[35]	53	54	AD[34]
AD[33]	55	56	Ground
V(I/O)	57	58	AD[32]
PCI-RSVD	59	60	PCI-RSVD
PCI-RSVD	61	62	Ground
Ground	63	64	PCI-RSVD

Table 2-3: PMC1 and PMC2 Connector Jn4 Rear I/O Pinouts

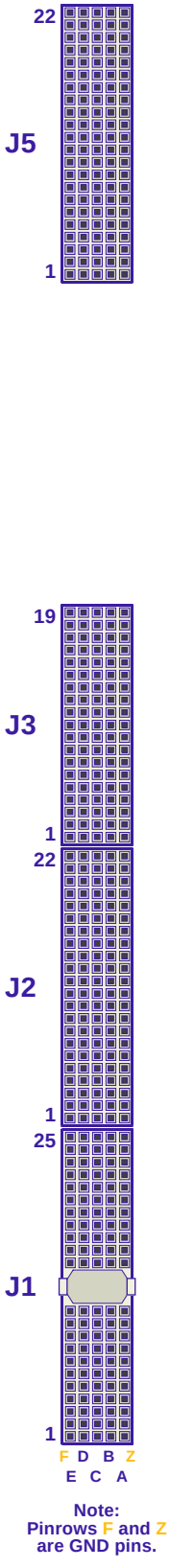
Jn4 (J14)				Jn4 (J24)			
SIGNAL	PIN	PIN	SIGNAL	SIGNAL	PIN	PIN	SIGNAL
PMC1IO1	1	2	PMC1IO2	PMC2IO1	1	2	PMC2IO2
PMC1IO3	3	4	PMC1IO4	PMC2IO3	3	4	PMC2IO4
PMC1IO5	5	6	PMC1IO6	PMC2IO5	5	6	PMC2IO6
PMC1IO7	7	8	PMC1IO8	PMC2IO7	7	8	PMC2IO8
PMC1IO9	9	10	PMC1IO10	PMC2IO9	9	10	PMC2IO10
PMC1IO11	11	12	PMC1IO12	PMC2IO11	11	12	PMC2IO12
PMC1IO13	13	14	PMC1IO14	PMC2IO13	13	14	PMC2IO14
PMC1IO15	15	16	PMC1IO16	PMC2IO15	15	16	PMC2IO16
PMC1IO17	17	18	PMC1IO18	PMC2IO17	17	18	PMC2IO18
PMC1IO19	19	20	PMC1IO20	PMC2IO19	19	20	PMC2IO20
PMC1IO21	21	22	PMC1IO22	PMC2IO21	21	22	PMC2IO22
PMC1IO23	23	24	PMC1IO24	PMC2IO23	23	24	PMC2IO24
PMC1IO25	25	26	PMC1IO26	PMC2IO25	25	26	PMC2IO26
PMC1IO27	27	28	PMC1IO28	PMC2IO27	27	28	PMC2IO28
PMC1IO29	29	30	PMC1IO30	PMC2IO29	29	30	PMC2IO30
PMC1IO31	31	32	PMC1IO32	PMC2IO31	31	32	PMC2IO32
PMC1IO33	33	34	PMC1IO34	PMC2IO33	33	34	PMC2IO34
PMC1IO35	35	36	PMC1IO36	PMC2IO35	35	36	PMC2IO36
PMC1IO37	37	38	PMC1IO38	PMC2IO37	37	38	PMC2IO38
PMC1IO39	39	40	PMC1IO40	PMC2IO39	39	40	PMC2IO40
PMC1IO41	41	42	PMC1IO42	PMC2IO41	41	42	PMC2IO42
PMC1IO43	43	44	PMC1IO44	PMC2IO43	43	44	PMC2IO44
PMC1IO45	45	46	PMC1IO46	PMC2IO45	45	46	PMC2IO46
PMC1IO47	47	48	PMC1IO48	PMC2IO47	47	48	PMC2IO48
PMC1IO49	49	50	PMC1IO50	PMC2IO49	49	50	PMC2IO50
PMC1IO51	51	52	PMC1IO52	PMC2IO51	51	52	PMC2IO52
PMC1IO53	53	54	PMC1IO54	PMC2IO53	53	54	PMC2IO54
PMC1IO55	55	56	PMC1IO56	PMC2IO55	55	56	PMC2IO56
PMC1IO57	57	58	PMC1IO58	PMC2IO57	57	58	PMC2IO58
PMC1IO59	59	60	PMC1IO60	PMC2IO59	59	60	PMC2IO60
PMC1IO61	61	62	PMC1IO62	PMC2IO61	61	62	PMC2IO62
PMC1IO63	63	64	PMC1IO64	PMC2IO63	63	64	PMC2IO64

Note ...

The PMC rear I/O signals from Jn4 (J14 and J24) are routed to CompactPCI connectors J3 and J5, whose pinout is described later in this chapter.

2.1.2 CompactPCI Bus Connector

Figure 2-2: CompactPCI Connectors J1, J2, J3, and J5



The CompactPCI interface provides all the necessary signals for data transfer as defined by the PCI Specification Rev. 2.1.

The CP690HS is connected to the CompactPCI backplane using the Pericom PI7C8154B PCI-to-PCI bridge, which interfaces the board with a data path width of 32 or 64-bit and a speed up to 33/66MHz. All bus signals are provided on the CompactPCI connectors J1 and J2 (64-bit extension). In addition to meeting the requirements of the interface definition of the CompactPCI Specification PICMG 2.0 R2.1, the CP690HS is designed to comply with the CompactPCI Hot Swap specification PICMG 2.1 R1.0, a consequence of which is that the CompactPCI interface of the board will be precharged when the board is plugged into a running system.

The complete CompactPCI connector configuration comprises four connectors named J1, J2, J3, and J5. Their functions are as follows:

- J1 and J2: 32/64-bit CompactPCI interface with PCI bus signals, arbitration, clock and power
- J3 and J5 have rear I/O interface functionality from the PMC module

The CP690HS is designed for a CompactPCI bus architecture. The CompactPCI standard is electrically identical to the PCI local bus. However, these systems are enhanced to operate in rugged industrial environments and to support multiple slots.

2.1.2.1 CompactPCI Connector Keying

The CompactPCI connectors support guide lugs to ensure a correct polarized mating.

The CP690HS supports universal CompactPCI VI/O signaling voltages with one common termination resistor configuration and includes a CompactPCI VI/O voltage detection circuit. If the CompactPCI VI/O voltage is 5 V, the maximum supported CompactPCI frequency is 33 MHz.

2.1.2.2 Hot Swap Support

To ensure that a board may be removed and replaced in a working bus without disturbing the system, the following additional features are required:

- Power ramping
- Precharge
- Hot swap control and status register bits
- Automatic interrupt generation whenever a board is about to be removed or replaced
- An LED to indicate that the board may be safely removed

For further information regarding the hot swap capability of the CP690HS, refer to Chapter 5.2, “Design Implementation on CP690HS”.

2.1.2.3 CompactPCI Connectors J1 and J2 Pinouts

The CP690HS is provided with two 2 mm x 2 mm pitch female CompactPCI bus connectors, J1 and J2. The different pin lengths are related to the hot swap functionality. For further information on the hot swap functionality, refer to section 5.1.1.1, “The Hot Swap Backplane”.

Table 2-4: CompactPCI Bus Connector J1 Pinout

PIN	ROW Z	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	GND	3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	NC	NC	GND	PERR#	GND
16	GND	DEVSEL#	PCIXCAP	V(I/O)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
14 - 12	Key Area						
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND
5	GND	NC	NC	PCI_RST#	GND	GNT#	GND
4	GND	NC	HEALTHY#	V(I/O)	NC	NC	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	NC	5V	NC	TDO	TDI	GND
1	GND	5V	-12V	NC	+12V	5V	GND

long pins (early power signals)

short pins (control signals)

medium-length pins

All signal names indicated in the table below refer to medium-length pins.

Table 2-5: CompactPCI Bus Connector J2 Pinout

PIN	ROW Z	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
22	GND	NC	NC	NC	NC	NC	GND
21	GND	NC	GND	NC	NC	NC	GND
20	GND	NC	GND	NC	GND	NC	GND
19	GND	GND	GND	NC	NC	NC	GND
18	GND	NC	NC	NC	GND	NC	GND
17	GND	NC	GND	NC	NC	NC	GND
16	GND	NC	NC	NC	GND	NC	GND
15	GND	NC	GND	NC	NC	NC	GND
14	GND	AD35#	AD34#	AD33#	GND	AD32#	GND
13	GND	AD38#	GND	V(I/O)	AD37#	AD36#	GND
12	GND	AD42#	AD41#	AD40#	GND	AD39#	GND
11	GND	AD45#	GND	V(I/O)	AD44#	AD43#	GND
10	GND	AD49#	AD48#	AD47#	GND	AD46#	GND
9	GND	AD52#	GND	V(I/O)	AD51#	AD50#	GND
8	GND	AD56#	AD55#	AD54#	GND	AD53#	GND
7	GND	AD59#	GND	V(I/O)	AD58#	AD57#	GND
6	GND	AD63#	AD62#	AD61#	GND	AD60#	GND
5	GND	C/BE5	64EN#	V(I/O)	C/BE4#	PAR64	GND
4	GND	V(I/O)	NC	C/BE7#	GND	C/BE6#	GND
3	GND	NC	GND	NC	NC	NC	GND
2	GND	NC	NC	NC	NC	NC	GND
1	GND	NC	GND	NC	NC	NC	GND

medium-length pins

2.1.2.4 CompactPCI Rear I/O Connectors J3 and J5 and Pinouts

The CP690HS conducts all PMC signals through the rear I/O connectors J3 and J5. The CP690HS board provides optional rear I/O connectivity for peripherals.

For the rear I/O feature, a suitable backplane is necessary which must be compliant with the CompactPCI Specification PICMG 2.0 R3.0, October 1999. The pinout of the CompactPCI rear I/O connectors J3 and J5 is compatible with all standard 6U CompactPCI passive backplanes with rear I/O support.

Table 2-6: CompactPCI Rear I/O Connector J3 Pinout

PIN	ROW Z	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
19	GND	NC	NC	NC	NC	NC	GND
18	GND	NC	NC	NC	NC	NC	GND
17	GND	NC	NC	NC	NC	NC	GND
16	GND	NC	NC	NC	NC	NC	GND
15	GND	NC	NC	NC	NC	NC	GND
14	GND	RIO_3.3V	RIO_3.3V	RIO_3.3V	RIO_5V	RIO_5V	GND
13	GND	PMC1IO5	PMC1IO4	PMC1IO3	PMC1IO2	PMC1IO1	GND
12	GND	PMC1IO10	PMC1IO9	PMC1IO8	PMC1IO7	PMC1IO6	GND
11	GND	PMC1IO15	PMC1IO14	PMC1IO13	PMC1IO12	PMC1IO11	GND
10	GND	PMC1IO20	PMC1IO19	PMC1IO18	PMC1IO17	PMC1IO16	GND
9	GND	PMC1IO25	PMC1IO24	PMC1IO23	PMC1IO22	PMC1IO21	GND
8	GND	PMC1IO30	PMC1IO29	PMC1IO28	PMC1IO27	PMC1IO26	GND
7	GND	PMC1IO35	PMC1IO34	PMC1IO33	PMC1IO32	PMC1IO31	GND
6	GND	PMC1IO40	PMC1IO39	PMC1IO38	PMC1IO37	PMC1IO36	GND
5	GND	PMC1IO45	PMC1IO44	PMC1IO43	PMC1IO42	PMC1IO41	GND
4	GND	PMC1IO50	PMC1IO49	PMC1IO48	PMC1IO47	PMC1IO46	GND
3	GND	PMC1IO55	PMC1IO54	PMC1IO53	PMC1IO52	PMC1IO51	GND
2	GND	PMC1IO60	PMC1IO59	PMC1IO58	PMC1IO57	PMC1IO56	GND
1	GND	RIO_V(I/O)	PMC1IO64	PMC1IO63	PMC1IO62	PMC1IO61	GND

Warning!

The RIO_XXX signals are power supply **OUTPUTS** to supply the rear I/O module with power. These pins **MUST NOT** be connected to any other power source, either within the backplane itself or within a rear I/O module.

Failure to comply with the above will result in damage to your board.

Table 2-7: CompactPCI Rear I/O Connector J5 Pinout

PIN	ROW Z	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
22	GND	NC	NC	NC	NC	NC	GND
21	GND	NC	NC	NC	NC	NC	GND
20	GND	NC	NC	NC	NC	NC	GND
19	GND	NC	NC	NC	NC	NC	GND
18	GND	NC	NC	NC	NC	NC	GND
17	GND	NC	NC	NC	NC	NC	GND
16	GND	NC	NC	NC	NC	NC	GND
15	GND	NC	NC	NC	NC	NC	GND
14	GND	NC	NC	NC	NC	NC	GND
13	GND	PMC2IO5	PMC2IO4	PMC2IO3	PMC2IO2	PMC2IO1	GND
12	GND	PMC2IO10	PMC2IO9	PMC2IO8	PMC2IO7	PMC2IO6	GND
11	GND	PMC2IO15	PMC2IO14	PMC2IO13	PMC2IO12	PMC2IO11	GND
10	GND	PMC2IO20	PMC2IO19	PMC2IO18	PMC2IO17	PMC2IO16	GND
9	GND	PMC2IO25	PMC2IO24	PMC2IO23	PMC2IO22	PMC2IO21	GND
8	GND	PMC2IO30	PMC2IO29	PMC2IO28	PMC2IO27	PMC2IO26	GND
7	GND	PMC2IO35	PMC2IO34	PMC2IO33	PMC2IO32	PMC2IO31	GND
6	GND	PMC2IO40	PMC2IO39	PMC2IO38	PMC2IO37	PMC2IO36	GND
5	GND	PMC2IO45	PMC2IO44	PMC2IO43	PMC2IO42	PMC2IO41	GND
4	GND	PMC2IO50	PMC2IO49	PMC2IO48	PMC2IO47	PMC2IO46	GND
3	GND	PMC2IO55	PMC2IO54	PMC2IO53	PMC2IO52	PMC2IO51	GND
2	GND	PMC2IO60	PMC2IO59	PMC2IO58	PMC2IO57	PMC2IO56	GND
1	GND	RIO_V(I/O)	PMC2IO64	PMC2IO63	PMC2IO62	PMC2IO61	GND

Warning!

The RIO_XXX signals are power supply **OUTPUTS** to supply the rear I/O module with power. These pins **MUST NOT** be connected to any other power source, either within the backplane itself or within a rear I/O module.

Failure to comply with the above will result in damage to your board.

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Chapter 3

Installation

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3. Installation

The CP690HS has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

3.1 Safety Requirements

The following safety precautions must be observed when installing or operating the CP690HS. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

Caution!

If your board type is not specifically qualified as being hot swap capable, switch off the CompactPCI system power before installing the board in a free CompactPCI slot. Failure to do so could endanger your life or health and may damage your board or system.

Note ...

Certain CompactPCI boards require bus master and/or rear I/O capability. If you are in doubt whether such features are required for the board you intend to install, please check your specific board and/or system documentation to make sure that your system is provided with an appropriate free slot in which to insert the board.

ESD Equipment!

Your carrier board and PMC module contain electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

3.2 CP690HS Initial Installation Procedures

The following procedures are applicable only for the initial installation of the CP690HS in a system. Procedures for standard removal are found in their respective chapters.

To perform an initial installation of the CP690HS in a system proceed as follows:

1. Ensure that the safety requirements indicated Chapter 3.1 are observed.

Warning!

Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the CP690HS refer to Chapter 4. For the installation of CP690HS-specific peripheral devices and rear I/O devices, refer to the documentation provided with the device itself.

Warning!

Care must be taken when applying the procedures below to ensure that neither the CP690HS nor other system boards are physically damaged by the application of these procedures.

3. To install the CP690HS perform the following:
   1. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.
   2. Using the ejector handle, engage the board with the backplane. When the ejector handle is locked, the board is engaged.
   3. Fasten the front panel retaining screws.
   4. Connect all external interfacing cables to the board as required.
   5. Ensure that the board and all required interfacing cables are properly secured.
4. The CP690HS is now ready for operation. For operation of the CP690HS, refer to appropriate CP690HS-specific software, application, and system documentation.

3.3 Standard Removal Procedures

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed.

Warning!

Care must be taken when applying the procedures below to ensure that neither the CP690HS nor system boards are physically damaged by the application of these procedures.

2. Disconnect any interfacing cables that may be connected to the board.
3. Unscrew the front panel retaining screws.
4. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.
5. After disengaging the board from the backplane, pull the board out of the slot.
6. Dispose of the board as required.

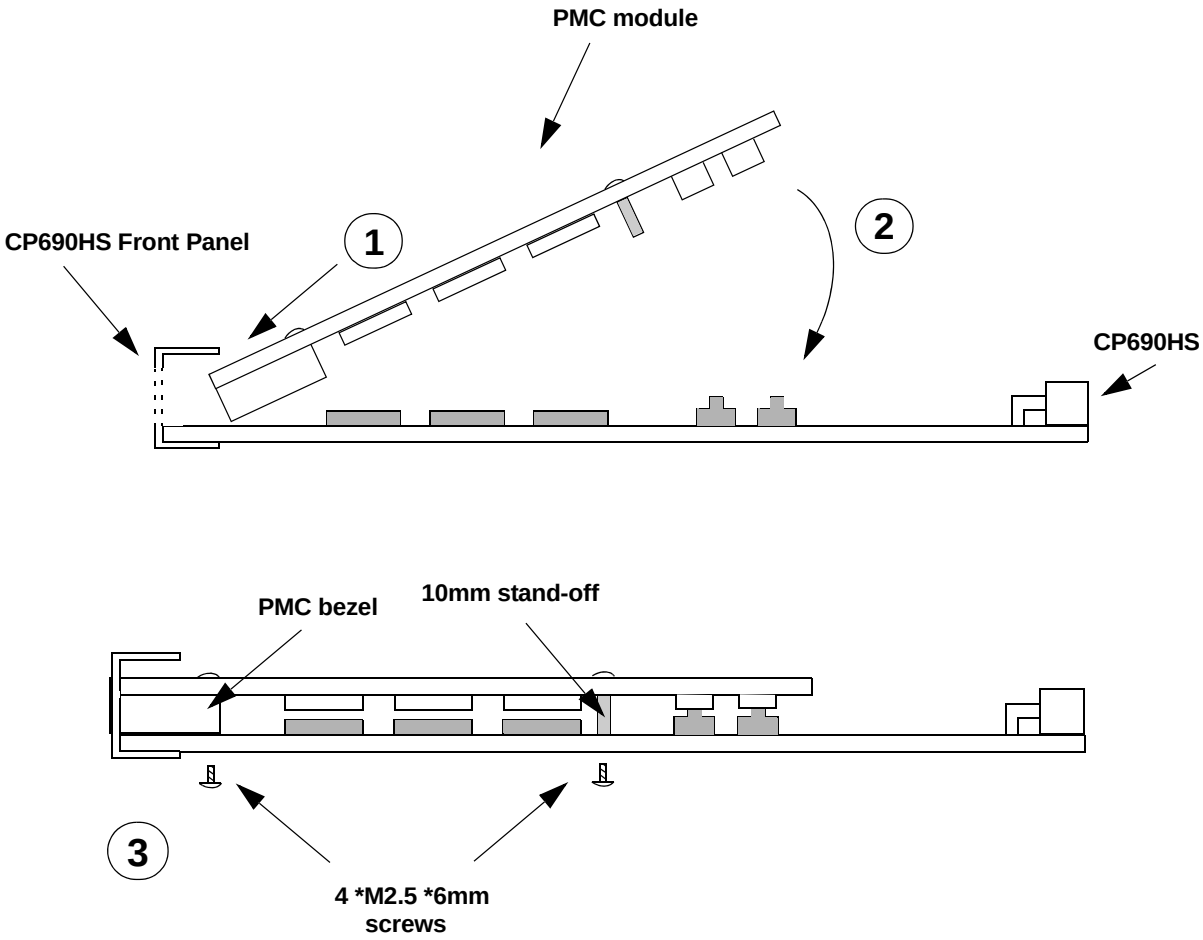
3.4 Installation of CP690HS Peripheral Devices

The CP690HS is designed to accommodate a variety of peripheral devices whose installation varies considerably. The following chapters provide information regarding installation aspects and not detailed procedures.

3.4.1 PMC Module Installation

1. Place the EMC gasket on the bezel of your PMC module.
2. Push the PMC bezel into the window of the front panel of the CP690HS and plug the connectors together.
3. Use four screws (M2.5 x 6mm) to fix the board.

Figure 3-1: Installation Diagram



Note ...

Only one key is present on each carrier board, either 3.3V or 5V, depending on the signaling used. The two PMC modules must both be set to the same voltage, i.e. either both 3.3V or both 5V.

3.4.1.1 CompactPCI Signaling Voltage

The primary side of the PCI-to-PCI bridge, i.e. the CompactPCI side, has buffers either for 3.3V or 5V signaling and is not selectable by the user.

3.4.1.2 PMC Signaling Voltage

The secondary (PMC) side of the PCI-to-PCI bridge may be configured either for a 3.3V or a 5V signaling environment. Please refer to Chapter 4, “Configuration” for jumper settings.

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Chapter 4

Configuration

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4. Configuration

4.1 Jumper Settings

The secondary side of the PCI-to-PCI bridge (the PMC side) may be configured either for a 3.3V or a 5V signalling environment. Configuration is effected by setting the jumpers (zero ohm resistors) R72 or R71.

Figure 4-1: Jumpers on the CP690HS

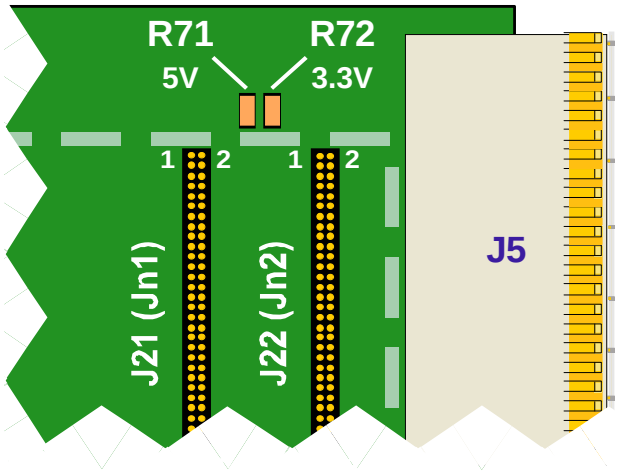

Table 4-1: Jumpers Settings

R72	R71	DESCRIPTION
Closed	*Open*	*3.3V signalling*
Open	*Closed*	5V signalling

The default setting is indicated by using italic bold.

Warning!

No other jumper settings are permitted as serious damage or misoperation will result.

Warning!

The PMC coding key must be set according to the chosen PMC voltage.

Care must be taken to ensure correct voltage configuration. Using an incorrect signalling voltage may damage the PMC module.

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Chapter 5

Hot Swap

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5. Hot Swap

5.1 Technical Background of CompactPCI Hot Swap

In many modern application systems downtime is costly and/or unacceptable. Server applications, telecommunications networks and automated systems requiring continuous monitoring call for a system design in which a single card can be inserted or extracted without affecting the rest of the system. The ease with which a board may be removed and replaced is dependent on the mechanical design (form factor), the possibility of deactivating the software drivers for the board (operating system) and the possibility of removing and inserting the board without disturbing the signal quality on the bus.

CompactPCI hot swap is currently the most effective way to meet this need. Staggered pins on the backplane guarantee controlled power sequencing of the board, while the signals ENUM, BDSEL, HEALTHY and the hot swap control and status register bits may be used to control board access from the software side.

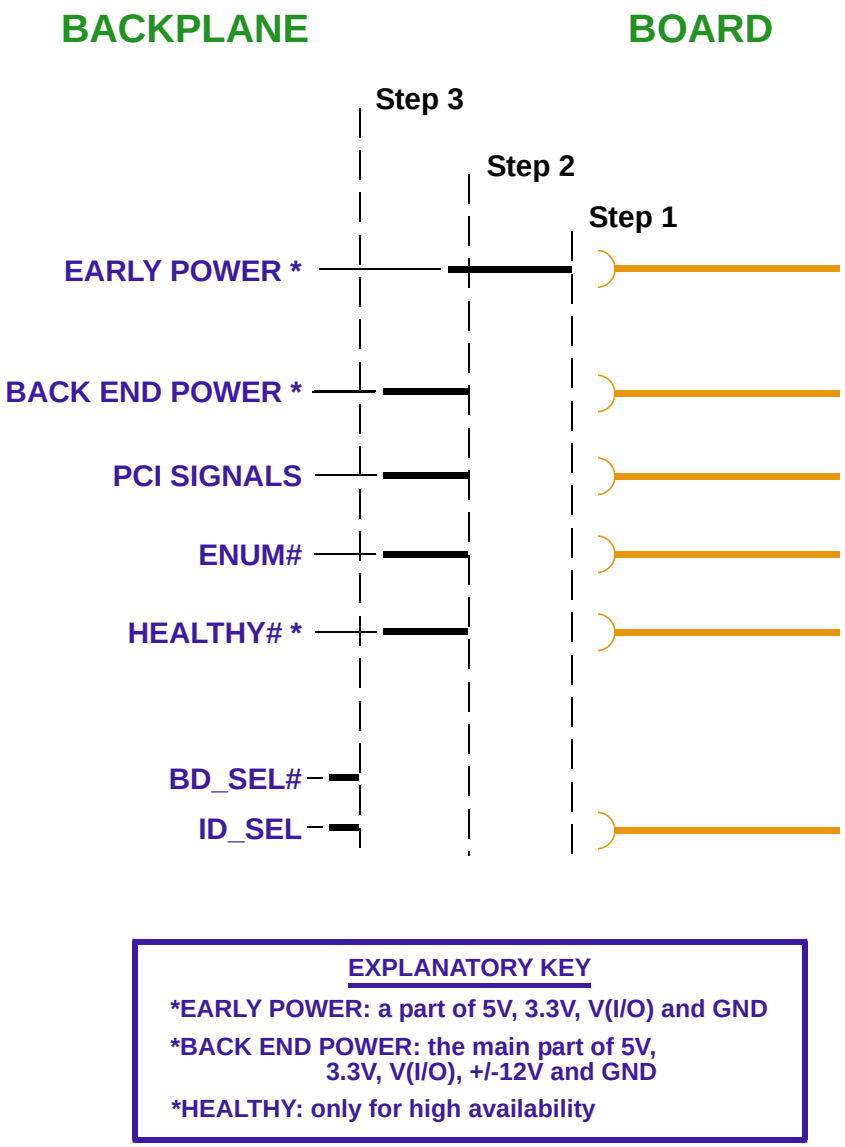
5.1.1 Hot Swap System

A hot swap system consists of a hot swap platform which comprises a hot swap backplane, the system host (CPU) with hot swap features, cooling, power supplies etc. plus the boards to be hot swapped. Hot swapping is not possible unless the operating system has the capability to enable and disable the board-specific driver during normal operation.

5.1.1.1 The Hot Swap Backplane

The hot swap backplane has staggered pins to ensure defined power sequencing.

Figure 5-1: Illustration of Staggered Pinning on the Hot Swap Backplane



Note ...

Some special signals (e.g. ENUM, HEALTHY, BDSEL, etc.) have particular routing requirements.

5.1.1.2 The System Host (System Controller)

The System Controller must have the possibility to utilize the special signals defined by the CompactPCI hot swap specification. If a high-availability system is used, it must additionally be able to control the hardware connection with the peripheral boards (Hardware Connection Control).

5.1.1.3 The Hot Swap Board

To ensure that a board may be removed and replaced in a working bus without disturbing the system it requires the following additional features:

- Precharge
- Power ramping
- Hot swap control and status register bits
- Automatic interrupt generation whenever a board is about to be removed or replaced.
- An LED to indicate that the board may be safely removed.

5.1.1.4 Software and Operating System

In a hot swap environment the software driver and the operating system have the following additional requirements:

- The OS must provide the possibility to initialize PCI devices during normal operation whenever required (allocate resources).
- The OS must provide the possibility to load or unload software drivers during normal operation whenever required.

5.2 Design Implementation on CP690HS

5.2.1 Power Ramping

On the CP690HS, a special hot swap controller is used to ramp up the supply voltage of the PMC modules (Back-End Power). This is done to avoid transients on the 3.3V and the 5V power supplies from the hot swap system. When the power supply is stable, the hot swap controller generates a reset on the PMC slots to put the devices into a definite state.

5.2.2 Precharge

Precharge is provided on the CP690HS by a resistor on each signal line (PCI bus), connected to a 1V reference voltage.

5.2.3 Handle Switch

A microswitch is situated in the extractor handle. Opening the handle initiates the generation of the ENUM interrupt (produced by the onboard logic).

5.2.4 ENUM# Interrupt

The onboard logic generates a low active interrupt signal to indicate that the board is about to be extracted from the system or inserted into the system.

5.2.5 Hot Swap Control and Status Register/Statemachine

All hot swap peripheral boards provide a Hot Swap Control and Status Register which provides information on the current state of the board. The defined bits in this register set are named, as follows:

Table 5-1: Hot Swap Control and Status Register / Statemachine

BIT	FUNCTION
EXT	Indication of extraction process
INS	Indication of insertion process
LOO	Led on
EIM	ENUM mask bit

These bits are implemented into the onboard logic. Since on-chip registers handle read and write accesses in the same way, it is necessary to exercise care when configuring the PCI-to-PCI GPIOs (General Purpose I/Os).

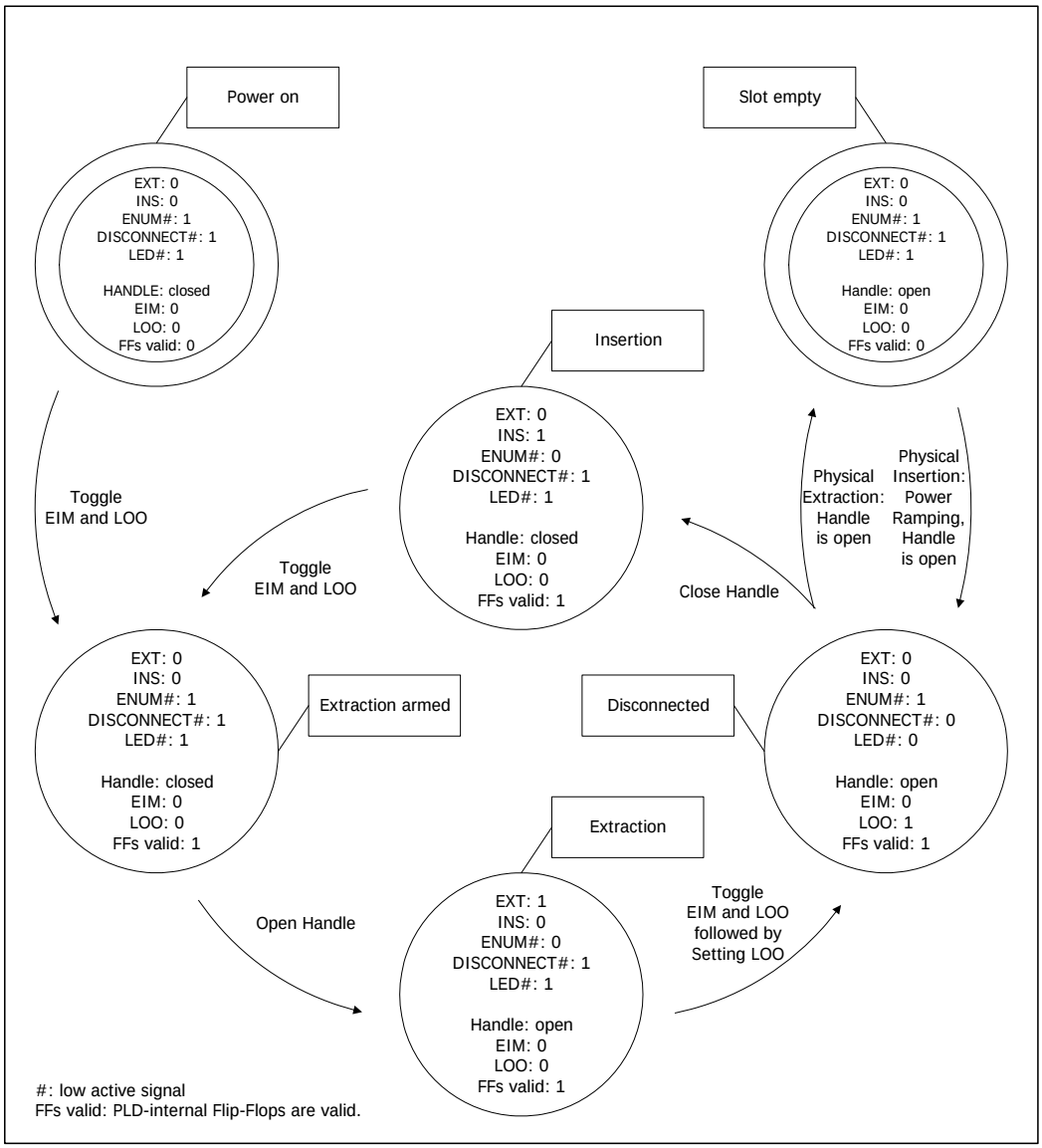
Table 5-2: Hot Swap Register Bits

BIT	SIGNAL ON PERICOM PI7C8154B
EXT	GPIO[2]
INS	GPIO[3]
LOO	GPIO[0]
EIM	GPIO[1]

Warning!

GPIO[2:3] have to be configured as inputs. A different configuration may damage your bridge device.

Figure 5-2: Hot Swap State Machine



5.2.6 Programming the GPIOs

This sub-chapter provides information for programming the GPIOs (General Purpose I/Os) of the PCI-to-PCI bridge.

5.2.6.1 GPIO: Output Enable Control Register - Offset 66h

This section describes the GPIO for the Output Enable Control Register.

Dword address = 64h

Byte enable p_cbe_1<3:0> = x0xxb

Table 5-3: GPIO Output Enable Control Register - Offset 66h

Dword BIT	NAME	R/W	DESCRIPTION
19:16	GPIO output enable write-1-to-clear	R/W1TC	The gpio<3:0> output enable control write-1-to-clear. Writing 1 to any of these bits configures the corresponding gpio<3:0> pin as an input only; that is, the output driver is tristated. Writing 0 to this register has no effect. When read, reflects the last value written. Reset value: 0 (all pins are input only).
23:20	GPIO output enable write-1-to-set	R/W1TS	The gpio<3:0> output enable control write-1-to-set. Writing 1 to any of these bits configures the corresponding gpio<3:0> pin as bidirectional, that is, enables the output driver and drives the value set in the output data register (65h). Writing 0 to this register has no effect. When read, reflects the last value written. Reset value: 0 (all pins are input only).

5.2.6.2 GPIO Input Data Register - Offset 67h

This section describes the GPIO input data register.

Dword address = 64h

Byte enable p_cbe_1<3:0> = 0xxxb

Table 5-4: GPIO Input Data Register - Offset 67h

Dword BIT	NAME	R/W	DESCRIPTION
27:24	Reserved	R	Reserved. Returns 0 when read.
31:28	GPIO input	R	This read-only register reads the state of the gpio<3:0> pins. This state is updated on the PCI clock cycle following a change in the gpio pins.

5.2.6.3 GPIO Output Data Register - Offset 65h

This section describes the GPIO output data register.

Dword address = 64h

Byte enable p_cbe_1<3:0> = xx0xb

Table 5-5: GPIO Output Data Register - Offset 65h

Dword BIT	NAME	R/W	DESCRIPTION
11:8	GPIO output enable write-1-to-clear	R/W1TC	The gpio<3:0> pin output data write-1-to-clear. Writing 1 to any of these bits drives the corresponding bit low on the gpio<3:0> bus if it is programmed as bi-directional. Data is driven on the PCI clock cycle following completion of the configuration write to this register. Bit positions corresponding to gpio pins that are programmed as input only are not driven. Writing 0 to these bits has no effect. When read, reflects the last value written. Reset value: 0.
15:12	GPIO output enable write-1-to-set	R/W1TS	The gpio<3:0> pin output data write-1- to-set. Writing 1 to any of these bits drives the corresponding bit high on the gpio<3:0> bus if it is programmed as bi-directional. Data is driven on the PCI clock cycle following completion of the configuration write to this register. Bit positions corresponding to gpio pins that are programmed as input only are not driven. Writing 0 to these bits has no effect. When read, reflects the last value written. Reset value: 0.

Chapter 6

Power Considerations

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6. Power Considerations

6.1 System Power

The considerations presented in the ensuing sections must be taken into account by system integrators when specifying the CP690HS system environment.

6.2 CP690HS Voltage Ranges

The CP690HS board itself has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The table below indicates the absolute maximum input voltage ratings that must not be exceeded. Power supplies to be used with the CP690HS should be carefully tested to ensure compliance with these ratings.

Table 6-1: Absolute Maximum Ratings

SUPPLY VOLTAGE	ABSOLUTE MAXIMUM RATINGS
3.3 V	3.6 V
5 V	5.5 V
+12 V	+14.0 V
-12 V	-14.0 V

Warning!

The maximum permitted voltage indicated in the table above must not be exceeded. Failure to comply with the above may result in damage to your board.

The following table specifies the ranges for the different input power voltages within which the board is functional. The CP690HS is not guaranteed to function if the board is not operated within the prescribed limits.

Table 6-2: DC Operational Input Voltage Ranges

INPUT SUPPLY VOLTAGE	ABSOLUTE RANGE	RECOMMENDED RANGE	REMARKS
3.3 V	3.2 V min. to 3.47 V max.	3.3 V min. to 3.47 V max.	Main voltage
5 V	4.85 V min. to 5.25 V max.	5.0 V min. to 5.25 V max.	Main voltage
+12 V	11.4 V min. to 12.6 V max.	12 V min. to 12.6 V max.	Not required
-12 V	-11.4 V min. to -12.6 V max.	-12 V min. to -12.6 V max.	Not required

6.3 Backplane Requirements

Backplanes to be used with the CP690HS must be adequately specified. The backplane must provide optimal power distribution for the 3.3 V, 5 V, +12 V and -12V power inputs. It is recommended to use only backplanes which have two power planes for the 3.3 V and 5 V voltages.

Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under-dimensioned cabling or bridges, high-resistance connections, etc. must be avoided. It is recommended to use POSITRONIC or M-type connector backplanes and power supplies where possible.

6.4 Power Supply Units

Power supplies for the CP690HS must be specified with enough reserve for the remaining system consumption. In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. An industrial power supply unit should be able to provide at least twice as much power as the entire system requires. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires.

As the design of the CP690HS has been optimized for minimal power consumption, the power supply unit shall be stable even without minimum load.

Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane. The power supply should be sufficient to allow for die resistance variations.

Note ...

Non-industrial ATX PSUs require a greater minimum load than a single CP690HS is capable of creating. When a PSU of this type is used, it will not power up correctly and the CP690HS may hang up. The solution is to use an industrial PSU or to add more load to the system.

If DC/DC power supplies are used, please ensure that the external main supply provides sufficient power in order to start-up the system properly. The external main supply should provide at least as much power as the system power supply is able to provide taking into consideration the inrush current.

Warning!

An under-dimensioned power supply may cause damage to system components.

The start-up behavior of CompactPCI and PCI (ATX) power supplies is critical for all new CompactPCI boards. These boards require a defined power of sequence and start-up behavior of the power supply. For information on the required behavior refer to the power supply specifications on the formfactors.org web site and to the CompactPCI (PICMG) specification on the picmgeu.org web site.

6.4.1 Voltage Ramp

Power supplies must comply with the following guidelines, in order to be used with the CP690HS.

- Beginning at 10% of the nominal output voltage, the voltage must rise within > 0.1 ms to < 20 ms to the specified regulation range of the voltage. Typically: > 5 ms to < 15 ms.
- There must be a smooth and continuous ramp of each DC output voltage from 10% to 90% of the regulation band.
- The slope of the turn-on waveform shall be a positive, almost linear voltage increase and have a value from 0 V to nominal Vout.

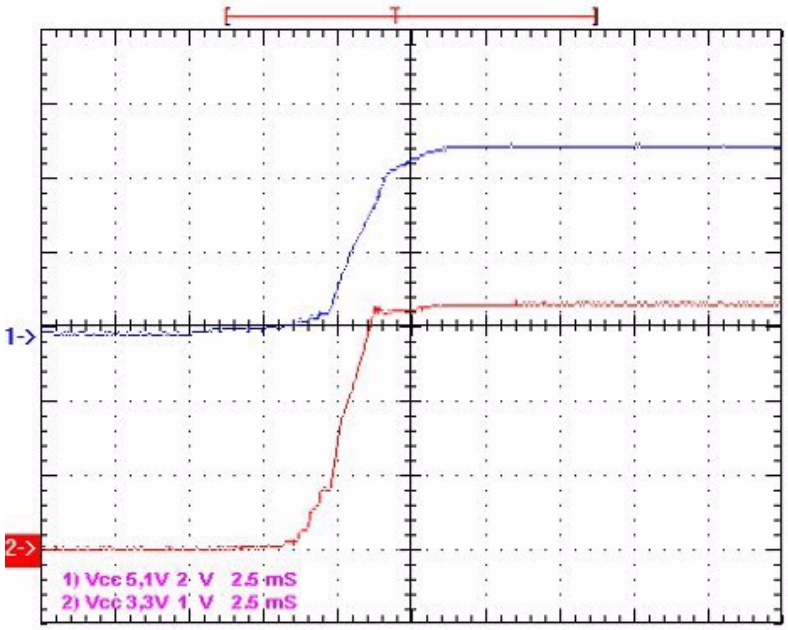
6.4.2 Voltage Sequencing Requirements

The 5 VDC output level must always be equal to or higher than the 3.3 VDC output during power-up and normal operation.

6.4.3 Rise Time Diagram

The following figure illustrates an example of the recommended voltage ramp of a CompactPCI power supply for all Kontron boards delivered up to now.

Figure 6-1: Voltage Ramp of the CP3-SVE180 AC Power Supply



6.4.4 Recommended Operating Conditions

The tolerance of the voltage lines is described in the CompactPCI specification (PICMG 2.0 R3.0).The recommended measurement point for the voltage is the CompactPCI connector on the CP690HS.

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No voltage of reverse polarity may be present on any output during turn-on or turn-off.

The following table provides information regarding the required characteristics for each board input voltage.

Table 6-3: Input Voltage Characteristics

VOLTAGE	NOMINAL VALUE	TOLERANCE	MAX. RIPPLE (p-p)
5 V	5.0 VDC	+5%/-3%	50 mV
3.3 V	3.3 VDC	+5%/-3%	50 mV
+12 V	+12 VDC	+5%/-5%	240 mV
-12 V	-12 VDC	+5%/-5%	240 mV
VI/O (PCI signaling voltage)	3.3 VDC or 5 VDC	+5%/-3%	50 mV
GND	Ground, not directly connected to protective earth (PE)		

6.4.5 Supply Voltage Regulation

The power supply shall be unconditionally stable under line, load, unload and transient load conditions including capacitive loads. The operation of the power supply must be consistent even without the minimum load on all output lines.

Note ...

Non-industrial ATX PSUs require a greater minimum load than a single CP690HS is capable of creating. When a PSU of this type is used, it will not power up correctly and the CP690HS may hang up. The solution is to use an industrial PSU or to add more load to the system.

Note ...

If the main power input is switched off, the supply voltages will not go to 0V instantly. It will take a couple of seconds until capacitors are discharged. If the voltage rises again before it has gone below a certain level, the circuits may enter a latch-up state where even a hard RESET will not help any more. The system must be switched off for at least 3 seconds before it may be switched on again. If problems still occur, turn off the main power for 30 seconds before turning it on again.

6.5 Power Consumption of the CP690HS

The goal of this description is to provide a method to calculate the power consumption for the CP690HS and additional PMC/PIM modules.

Table 6-4: Power Consumption CP690HS without PMC/PIM Module

POWER	CP690HS WITHOUT PMC/PIM MODULE
5 V	max. 1.2 W
3.3 V	max. 2.7 W

For further information on the power consumption of the CP690HS, please contact Kontron.

6.6 Maximum Allowable Power Consumption of PMC Modules

The following table indicates the total power consumption of both PMC modules that is permitted in order to be used on the CP690HS. Overcurrent security for the PMC modules is provided by the power controller.

Table 6-5: Maximum Allowable Power Consumption of Both PMC Modules

POWER	POWER CONSUMPTION OF BOTH PMC MODULES	
	MAX. POWER CONSUMPTION RANGE	TYPICAL POWER CONSUMPTION
5 V	4.0 A - 6.0 A	5.0 A
3.3 V	4.0 A - 6.0 A	5.0 A

Note ...

An extremely high inrush current of the PMC modules can lead to system instability or improper operation.

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Chapter 7

System Considerations

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7. System Considerations

It is the responsibility of the system integrator to ensure that sufficient air flow or cooling is provided for proper operation of the CP690HS and associated PMC modules.

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Appendix A

CP-RIO6-90

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A. CP-RIO6-90

A.1 Introduction

The CP-RIO6-90 rear I/O transition module has been designed for use only with the CP690HS 6U CompactPCI board from Kontron and enables the user to connect up to two PIM modules to the CP690HS.

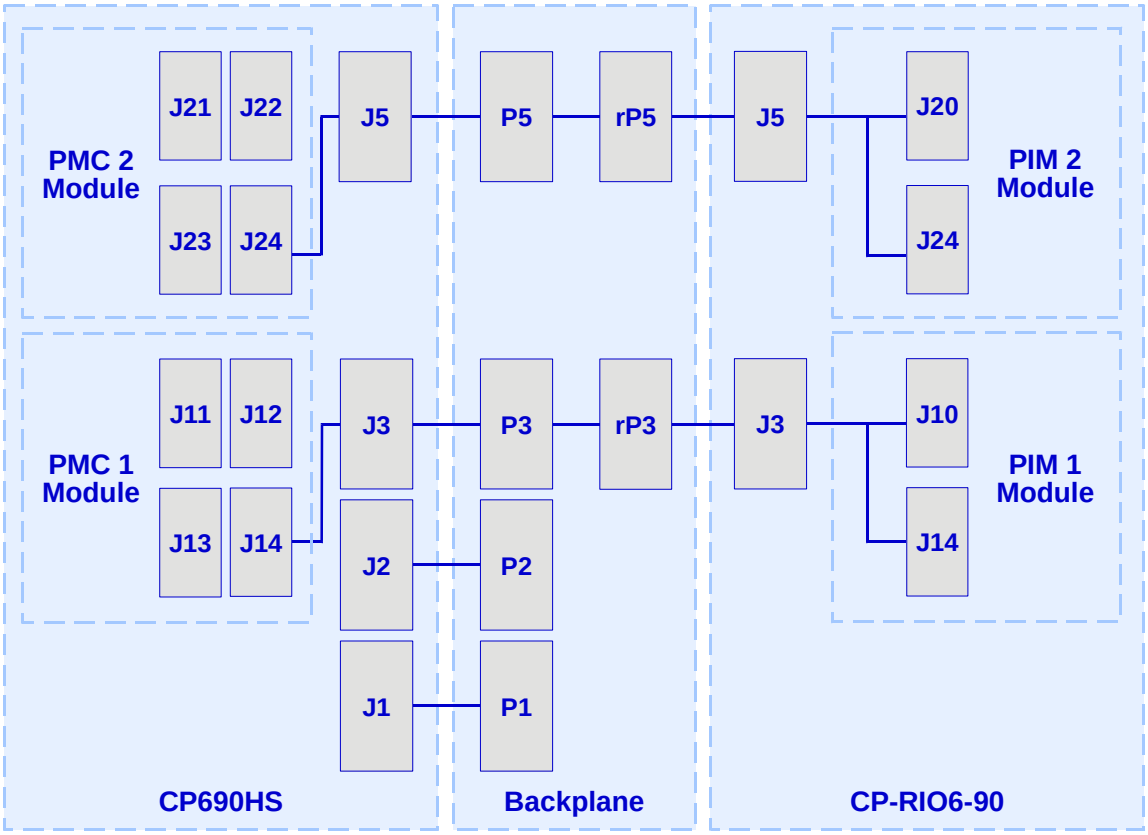
The CP-RIO6-90 is plugged in from the back of the system into the backplane connectors rP3 and rP5 in line with the CP690HS.

Note ...

The CP-RIO6-90 can be used only with the CP690HS hardware index 01 or higher (new rear I/O pinout), it cannot be used with the hardware index 00.

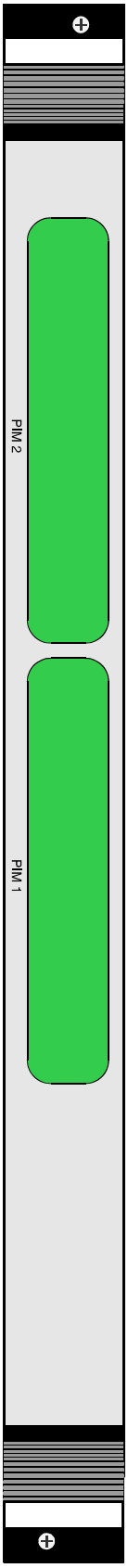
A.2 Functional Block Diagram

Figure A-1: CP-RIO6-90 Functional Block Diagram



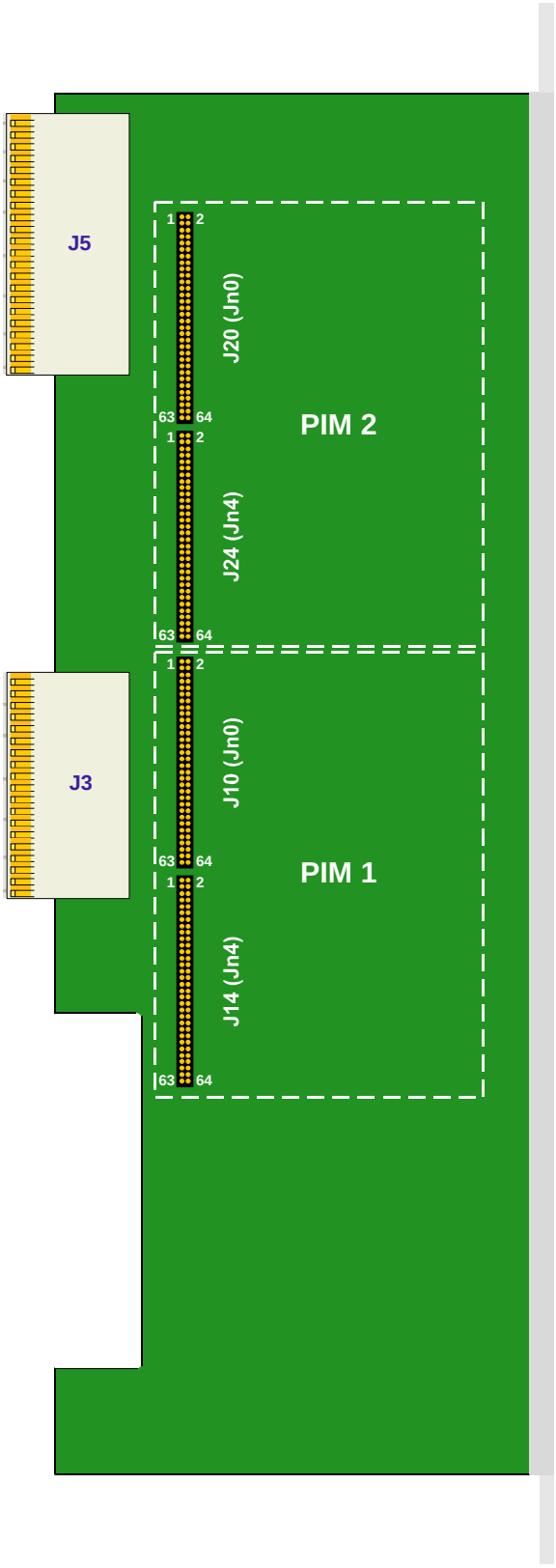
A.3 CP-RIO6-90 Front Panel

Figure A-2: CP-RIO6-90 Front Panel



A.4 CP-RIO6-90 Board Layout

Figure A-3: CP-RIO6-90 Board Layout



A.5 Module Interfaces

A.5.1 PIM Interfaces

Up to two PIM modules can be connected to the CP-RIO6-90 via the four 64-pin, female connectors J10, J14, J20, J24. The following tables indicate the pinouts of the PIM connectors.

Table A-1: PIM1 Connectors Jn0 (J10) and Jn4 (J14) Pinouts

Jn0 (J10)				Jn4 (J14)			
SIGNAL	PIN	PIN	SIGNAL	SIGNAL	PIN	PIN	SIGNAL
NC	1	2	NC	PIM1[01]	1	2	PIM1[02]
NC	3	4	NC	PIM1[03]	3	4	PIM1[04]
RIO_5V	5	6	NC	PIM1[05]	5	6	PIM1[06]
NC	7	8	NC	PIM1[07]	7	8	PIM1[08]
NC	9	10	RIO_3.3V	PIM1[09]	9	10	PIM1[10]
NC	11	12	NC	PIM1[11]	11	12	PIM1[12]
GND	13	14	NC	PIM1[13]	13	14	PIM1[14]
NC	15	16	NC	PIM1[15]	15	16	PIM1[16]
NC	17	18	GND	PIM1[17]	17	18	PIM1[18]
NC	19	20	NC	PIM1[19]	19	20	PIM1[20]
RIO_5V	21	22	NC	PIM1[21]	21	22	PIM1[22]
NC	23	24	NC	PIM1[23]	23	24	PIM1[24]
NC	25	26	RIO_3.3V	PIM1[25]	25	26	PIM1[26]
NC	27	28	NC	PIM1[27]	27	28	PIM1[28]
GND	29	30	NC	PIM1[29]	29	30	PIM1[30]
NC	31	32	NC	PIM1[31]	31	32	PIM1[32]
NC	33	34	GND	PIM1[33]	33	34	PIM1[34]
NC	35	36	NC	PIM1[35]	35	36	PIM1[36]
RIO_5V	37	38	NC	PIM1[37]	37	38	PIM1[38]
NC	39	40	NC	PIM1[39]	39	40	PIM1[40]
NC	41	42	RIO_3.3V	PIM1[41]	41	42	PIM1[42]
NC	43	44	NC	PIM1[43]	43	44	PIM1[44]
GND	45	46	NC	PIM1[45]	45	46	PIM1[46]
NC	47	48	NC	PIM1[47]	47	48	PIM1[48]
NC	49	50	GND	PIM1[49]	49	50	PIM1[50]
NC	51	52	NC	PIM1[51]	51	52	PIM1[52]
RIO_5V	53	54	NC	PIM1[53]	53	54	PIM1[54]
NC	55	56	NC	PIM1[55]	55	56	PIM1[56]
NC	57	58	RIO_3.3V	PIM1[57]	57	58	PIM1[58]
NC	59	60	NC	PIM1[59]	59	60	PIM1[60]
NC	61	62	NC	PIM1[61]	61	62	PIM1[62]
NC	63	64	NC	PIM1[63]	63	64	PIM1[64]

Table A-2: PIM2 Connectors Jn0 (J20) and Jn4 (J24) Pinouts

Jn0 (J20)				Jn4 (J24)			
SIGNAL	PIN	PIN	SIGNAL	SIGNAL	PIN	PIN	SIGNAL
NC	1	2	NC	PIM2[01]	1	2	PIM2[02]
NC	3	4	NC	PIM2[03]	3	4	PIM2[04]
RIO_5V	5	6	NC	PIM2[05]	5	6	PIM2[06]
NC	7	8	NC	PIM2[07]	7	8	PIM2[08]
NC	9	10	RIO_3.3V	PIM2[09]	9	10	PIM2[10]
NC	11	12	NC	PIM2[11]	11	12	PIM2[12]
GND	13	14	NC	PIM2[13]	13	14	PIM2[14]
NC	15	16	NC	PIM2[15]	15	16	PIM2[16]
NC	17	18	GND	PIM2[17]	17	18	PIM2[18]
NC	19	20	NC	PIM2[19]	19	20	PIM2[20]
RIO_RIO_	21	22	NC	PIM2[21]	21	22	PIM2[22]
NC	23	24	NC	PIM2[23]	23	24	PIM2[24]
NC	25	26	RIO_RIO_	PIM2[25]	25	26	PIM2[26]
NC	27	28	NC	PIM2[27]	27	28	PIM2[28]
GND	29	30	NC	PIM2[29]	29	30	PIM2[30]
NC	31	32	NC	PIM2[31]	31	32	PIM2[32]
NC	33	34	GND	PIM2[33]	33	34	PIM2[34]
NC	35	36	NC	PIM2[35]	35	36	PIM2[36]
RIO_5V	37	38	NC	PIM2[37]	37	38	PIM2[38]
NC	39	40	NC	PIM2[39]	39	40	PIM2[40]
NC	41	42	RIO_3.3V	PIM2[41]	41	42	PIM2[42]
NC	43	44	NC	PIM2[43]	43	44	PIM2[44]
GND	45	46	NC	PIM2[45]	45	46	PIM2[46]
NC	47	48	NC	PIM2[47]	47	48	PIM2[48]
NC	49	50	GND	PIM2[49]	49	50	PIM2[50]
NC	51	52	NC	PIM2[51]	51	52	PIM2[52]
RIO_5V	53	54	NC	PIM2[53]	53	54	PIM2[54]
NC	55	56	NC	PIM2[55]	55	56	PIM2[56]
NC	57	58	RIO_3.3V	PIM2[57]	57	58	PIM2[58]
NC	59	60	NC	PIM2[59]	59	60	PIM2[60]
NC	61	62	NC	PIM2[61]	61	62	PIM2[62]
NC	63	64	NC	PIM2[63]	63	64	PIM2[64]

Warning!

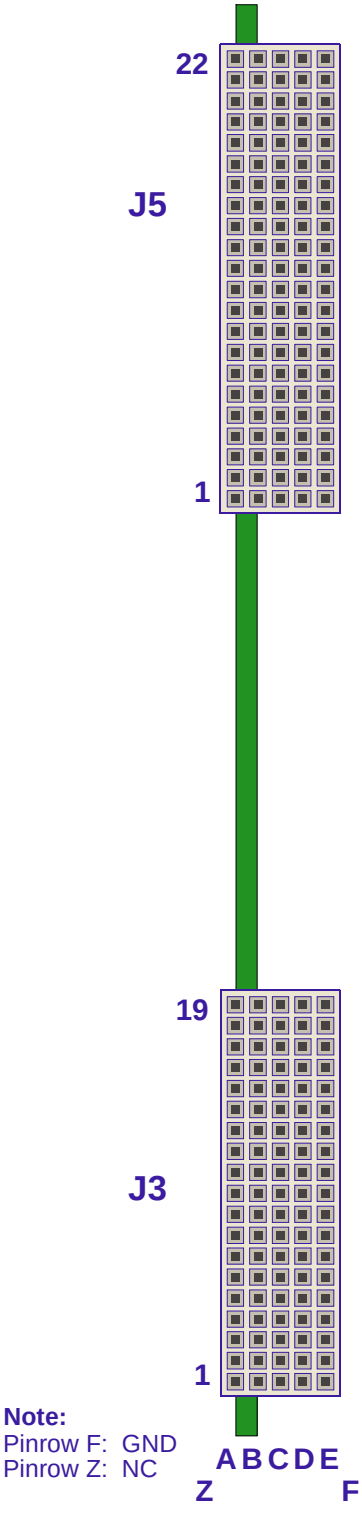
The RIO_XXX signals indicated in tables A-1 and A-2 are power supply **INPUTS** to supply the rear I/O module with power. These pins **MUST NOT** be connected to any other power source, either within the backplane itself or within a rear I/O module.

Failure to comply with the above will result in damage to your board.

A.5.2 CompactPCI Rear I/O Interface on the CP-RIO6-90 Module

The CP-RIO6-90 is equipped with two female CompactPCI rear I/O connectors, J3 and J5.

Figure A-4: CompactPCI Rear I/O Connectors J3 and J5



The following tables provide the pinouts of the CompactPCI rear I/O connectors, J3 and J5. The same pinouts apply to the matching rear I/O connectors rP3 and rP5 located on the backplane.

Table A-3: CompactPCI Rear I/O Connector J3 Pinout

PIN	Z	A	B	C	D	E	F
19	NC	RIO_5V	RIO_5V	RIO_3.3V	NC	NC	GND
18	NC	NC	NC	GND	NC	NC	NC
17	NC	NC	NC	GND	NC	NC	GND
16	NC	NC	NC	GND	NC	NC	NC
15	NC	NC	NC	GND	NC	NC-	GND
14	NC	RIO_3.3V	RIO_3.3V	RIO_3.3V	RIO_5V	NC	NC
13	NC	PMC1_IO[05]	PMC1_IO[04]	PMC1_IO[03]	PMC1_IO[02]	PMC1_IO[01]	GND
12	NC	PMC1_IO[10]	PMC1_IO[09]	PMC1_IO[08]	PMC1_IO[07]	PMC1_IO[06]	NC
11	NC	PMC1_IO[15]	PMC1_IO[14]	PMC1_IO[13]	PMC1_IO[12]	PMC1_IO[11]	GND
10	NC	PMC1_IO[20]	PMC1_IO[19]	PMC1_IO[18]	PMC1_IO[17]	PMC1_IO[16]	NC
9	NC	PMC1_IO[25]	PMC1_IO[24]	PMC1_IO[23]	PMC1_IO[22]	PMC1_IO[21]	GND
8	NC	PMC1_IO[30]	PMC1_IO[29]	PMC1_IO[28]	PMC1_IO[27]	PMC1_IO[26]	NC
7	NC	PMC1_IO[35]	PMC1_IO[34]	PMC1_IO[33]	PMC1_IO[32]	PMC1_IO[31]	GND
6	NC	PMC1_IO[40]	PMC1_IO[39]	PMC1_IO[38]	PMC1_IO[37]	PMC1_IO[36]	NC
5	NC	PMC1_IO[45]	PMC1_IO[44]	PMC1_IO[43]	PMC1_IO[42]	PMC1_IO[41]	GND
4	NC	PMC1_IO[50]	PMC1_IO[49]	PMC1_IO[48]	PMC1_IO[47]	PMC1_IO[46]	NC
3	NC	PMC1_IO[55]	PMC1_IO[54]	PMC1_IO[53]	PMC1_IO[52]	PMC1_IO[51]	GND
2	NC	PMC1_IO[60]	PMC1_IO[59]	PMC1_IO[58]	PMC1_IO[57]	PMC1_IO[56]	NC
1	NC	NC	PMC1_IO[64]	PMC1_IO[63]	PMC1_IO[62]	PMC1_IO[61]	GND

Warning!

The RIO_XXX signals are power supply **INPUTS** to supply the rear I/O module with power. These pins **MUST NOT** be connected to any other power source, either within the backplane itself or within a rear I/O module.

Failure to comply with the above will result in damage to your board.

Table A-4: CompactPCI Rear I/O Connector J5 Pinout

PIN	Z	A	B	C	D	E	F
22	NC	NC	NC	NC	NC	NC	NC
21	NC	NC	NC	NC	NC	NC	GND
20	NC	NC	NC	NC	NC	NC	NC
19	NC	NC	NC	NC	NC	NC	GND
18	NC	NC	NC	NC	NC	NC	NC
17	NC	NC	NC	NC	NC	NC	GND
16	NC	NC	NC	NC	NC	NC	NC
15	NC	NC	NC	NC	NC	NC	GND
14	NC	NC	NC	NC	NC	NC	NC
13	NC	PMC2_IO[05]	PMC2_IO[04]	PMC2_IO[03]	PMC2_IO[02]	PMC2_IO[01]	GND
12	NC	PMC2_IO[10]	PMC2_IO[09]	PMC2_IO[08]	PMC2_IO[07]	PMC2_IO[06]	NC
11	NC	PMC2_IO[15]	PMC2_IO[14]	PMC2_IO[13]	PMC2_IO[12]	PMC2_IO[11]	GND
10	NC	PMC2_IO[20]	PMC2_IO[19]	PMC2_IO[18]	PMC2_IO[17]	PMC2_IO[16]	NC
9	NC	PMC2_IO[25]	PMC2_IO[24]	PMC2_IO[23]	PMC2_IO[22]	PMC2_IO[21]	GND
8	NC	PMC2_IO[30]	PMC2_IO[29]	PMC2_IO[28]	PMC2_IO[27]	PMC2_IO[26]	NC
7	NC	PMC2_IO[35]	PMC2_IO[34]	PMC2_IO[33]	PMC2_IO[32]	PMC2_IO[31]	GND
6	NC	PMC2_IO[40]	PMC2_IO[39]	PMC2_IO[38]	PMC2_IO[37]	PMC2_IO[36]	NC
5	NC	PMC2_IO[45]	PMC2_IO[44]	PMC2_IO[43]	PMC2_IO[42]	PMC2_IO[41]	GND
4	NC	PMC2_IO[50]	PMC2_IO[49]	PMC2_IO[48]	PMC2_IO[47]	PMC2_IO[46]	NC
3	NC	PMC2_IO[55]	PMC2_IO[54]	PMC2_IO[53]	PMC2_IO[52]	PMC2_IO[51]	GND
2	NC	PMC2_IO[60]	PMC2_IO[59]	PMC2_IO[58]	PMC2_IO[57]	PMC2_IO[56]	NC
1	NC	NC	PMC2_IO[64]	PMC2_IO[63]	PMC2_IO[62]	PMC2_IO[61]	GND

A.6 Technical Specifications

Table A-5: CP-RIO6-90 Main Specifications

CP-RIO6-90		SPECIFICATIONS
External Interface	CompactPCI Rear I/O Interfaces	Two CompactPCI rear I/O connectors, J3 and J5
Internal Interfaces	PIM Interface	Four onboard, 64-pin, female PIM connectors: • PIM1: J10 and J14 • PIM2: J20 and J24
General	Power Consumption	3.3 V and 5.0 V: ≤100 mW (without PIM module)
	Temperature Range	Operating temp.: 0°C to +75°C
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	233.35 mm x 80 mm (6U rear I/O card size)
	Module Weight	200 grams (without PIM module)

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