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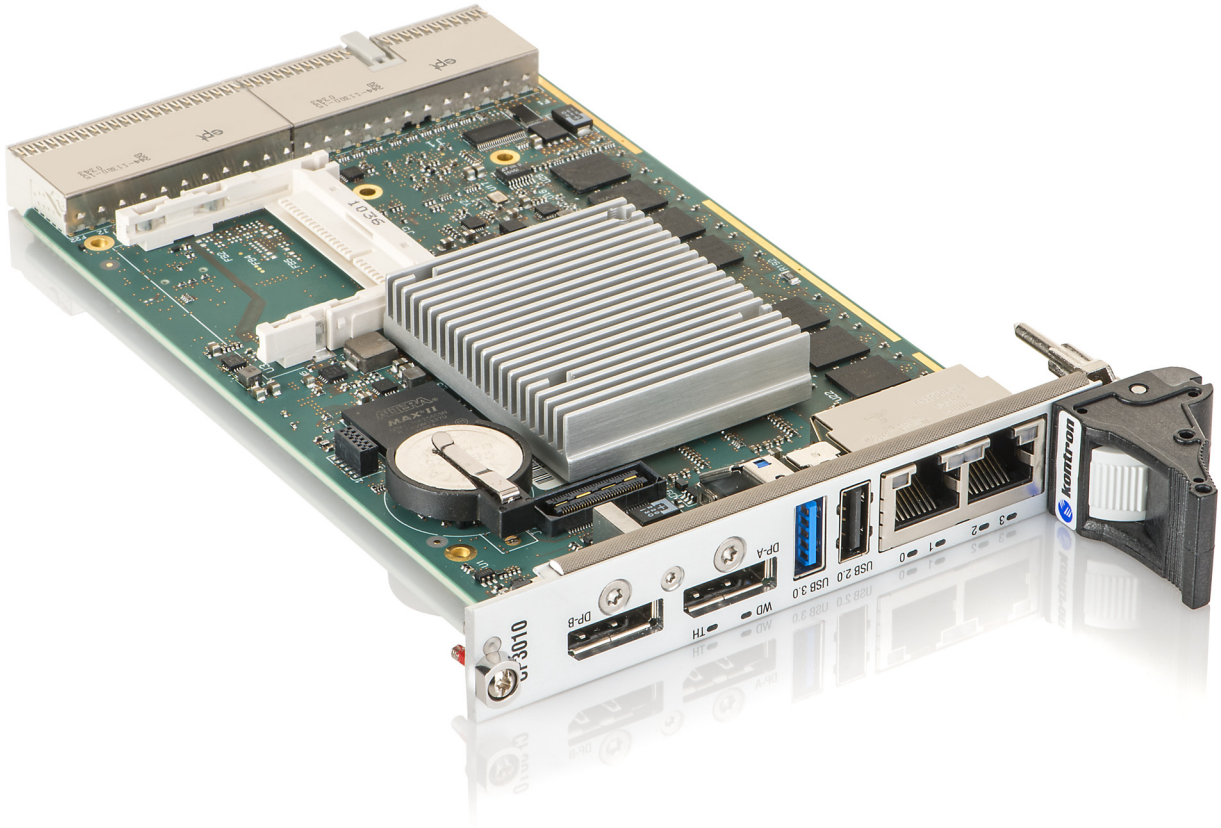

CP3010-SA

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Revision History

Revision	Brief Description of Changes	Date of Issue
1.0	Initial issue	4-Nov-2014
2.0	General update, made changes to Chapter 1.5 and Chapter 5.1	25-Aug-2016

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1 Introduction

1.1 Board Overview

The CP3010-SA is a highly integrated, low-power, 3U CompactPCI® CPU board designed to support the Intel® Atom™ processors E3845 and E3827 with a maximum of quad-core 1.91 GHz processing performance. Even though the board design is based on the Atom™ technology, performance levels of former Core™2 Duo platforms can be reached. Further, the built-in graphics core now features Intel® HD Graphics Technology offering an outstanding increase in graphics performance compared to previous Atom™ designs.

Memory demanding applications can make use of up to 8 GB soldered DDR3L SDRAM memory running at 1333 MHz. For onboard data storage, the CP3010-SA offers a CFast option or a soldered SATA Flash and, on the 8HP extension module, an HDD/SSD option. On the system side, the CP3010-SA supports a PCI 32-bit, 33 MHz (66 MHz on request) CompactPCI® interface enabling the peripheral mode feature.

Using the latest Atom™ technology, the board offers a very low TDP (thermal design power) value. This feature, in conjunction with the special heat sink design, makes the CP3010-SA a perfect fit for all systems and applications where cooling by fans is not desired or not possible. As a result, operation in temperature ranges from -40°C up to +85°C is possible.

Designed with soldered processor and memory to handle even the toughest environmental conditions, the CP3010-SA can be used in industrial and mobile applications where motion, shock and vibration can typically be found. With respect to the transportation market, the CP3010-SA is fully EN50155-compliant.

The CP3010-SA comes with a comprehensive I/O feature set supporting interfaces such as DisplayPort, USB 3.0/2.0, Gigabit Ethernet, SATA, CAN, and RS-232 serial ports as well as the audio interfaces Line-In and Line-Out. Available as 4HP or 8HP version – optionally combined with rear I/O support – the CP3010-SA can be adapted to a wide range of application needs.

As a stable product based on Intel®‘s embedded product line, the CP3010-SA ensures long-term availability. This eliminates the risk of unplanned design changes and unexpected expensive application modification. While minimizing deployment risks by providing a broad range of software support, the CP3010-SA eases the process of product integration and maximizes competitive advantages to meet time-to-market windows.

The board is offered with various Board Support Packages including Windows, VxWorks and Linux operating systems. For further information concerning the operating systems available for the CP3010-SA, please contact Kontron.

1.2 System Expansion Capabilities

1.2.1 CP3010-HDD Extension Module (8 HP)

The CP3010-HDD extension module for the 8 HP CP3010-SA version provides onboard support for a 2.5" HDD/SSD and various ports on the front panel, such as one USB 2.0 port, one COM port, one Gigabit Ethernet, one CAN port, and two audio interfaces (Line-In and Line-Out). For further information on the CP3010-HDD extension module, refer to Chapter 6.

1.2.2 CP-RIO3-04 Rear Transition Module

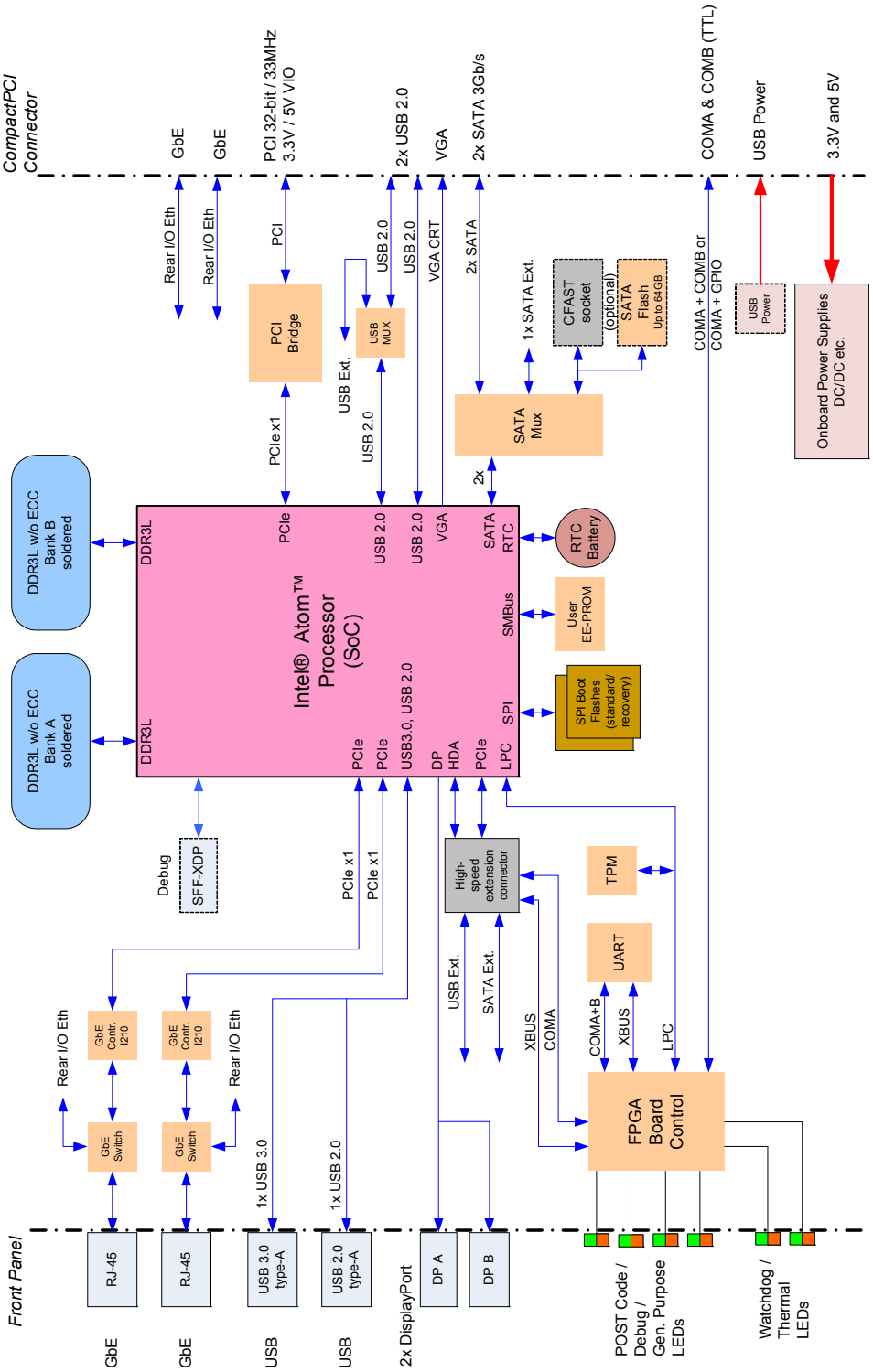
The CP-RIO3-04 rear transition module has been designed for use with the CP3010-SA and provides comprehensive rear I/O functionality. For further information on the CP-RIO3-04 rear transition module, refer to Chapter 7.

1.3 Board Diagrams

The following diagrams provide additional information concerning board functionality and component layout.

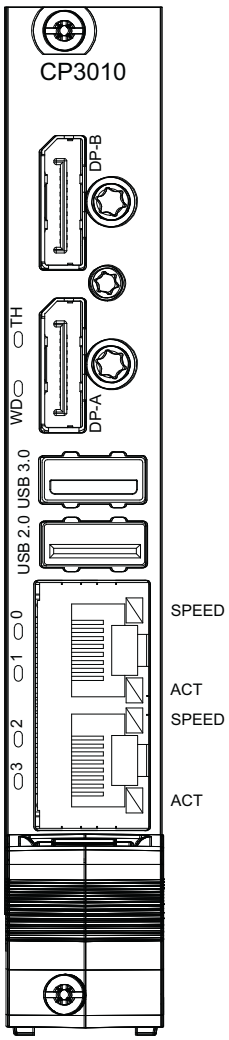
1.3.1 Functional Block Diagram

Figure 1: CP3010-SA Functional Block Diagram



1.3.2 Front Panel

Figure 2: 4 HP CP3010-SA Front Panel



System Status LEDs

TH (red/green): Temperature Status
WD (green): Watchdog Status

General Purpose LEDs

LED3..0 (red/green/red+green): General Purpose/ POST Code

Note: If the General Purpose LEDs 3..0 are lit red during boot-up, a failure is indicated before the uEFI BIOS has started.

Integral Ethernet LEDs

ACT (green): Ethernet Link/Activity
SPEED (orange): 1000BASE-T Ethernet Speed
SPEED (green): 100BASE-TX Ethernet Speed
SPEED (off) + ACT on: 10BASE-T Ethernet Speed

Note: For information regarding the front panel of the 8 HP CP3010-SA with a CP3010-HDD extension module, refer to Chapter 6.

1.3.3 Board Layout

Figure 3: 4 HP CP3010-SA Board Layout (Top View)

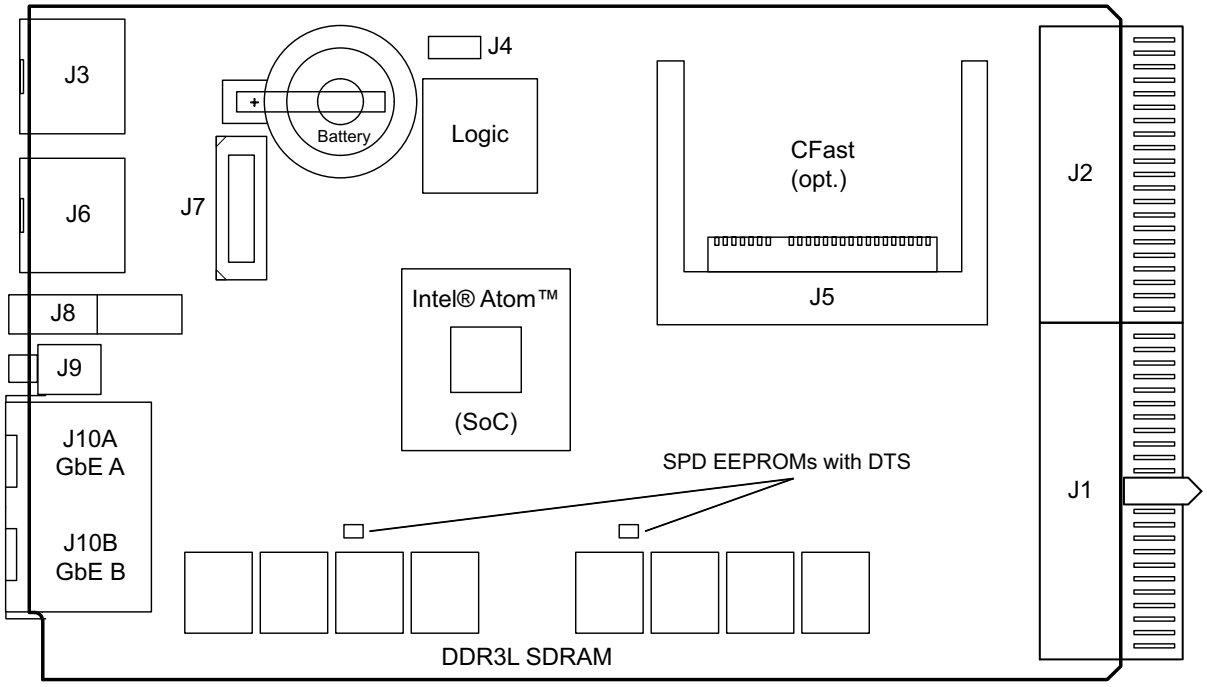
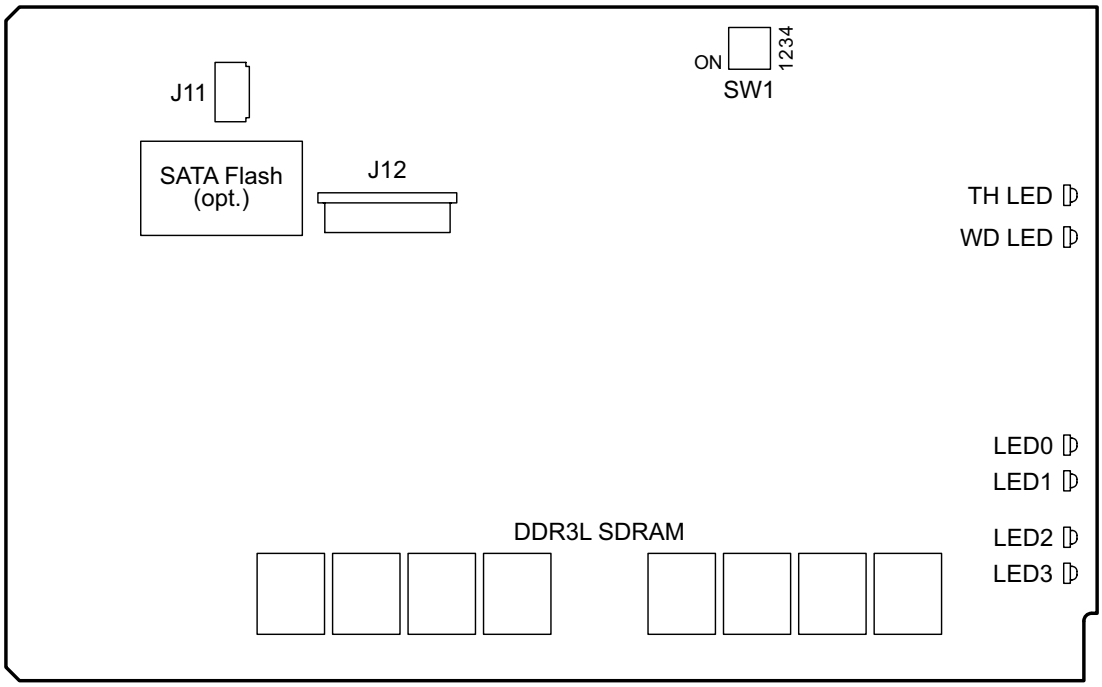


Figure 4: 4 HP CP3010-SA Board Layout (Bottom View)



1.4 Technical Specification

Table 1: CP3010-SA Main Specifications

FEATURES		SPECIFICATIONS
SoC	CPU	The CP3010-SA supports the following processors: » Quad-core Intel® Atom™ E3845, 1.91 GHz, 2 MB L2 cache » Dual-core Intel® Atom™ E3827, 1.75 GHz, 1 MB L2 cache
	Graphics Controller	Intel® HD Graphics integrated in the processor with support for two independent displays
Memory	Main Memory	Up to 8 GB, dual-channel DDR3L SDRAM memory without ECC running at 1333 MHz (soldered)
	Flash Memory	Two 8 MB SPI boot flash chips for two separate uEFI BIOS images SATA NAND flash (optional): » Up to 64 GB soldered SATA NAND flash, or » CFast card
	EEPROM	EEPROM with 64 kbit
Interfaces	CompactPCI	CompactPCI interface: » Compliant with CompactPCI Specification PICMG® 2.0 R 3.0 » System master operation » 32-bit / 33 MHz master interface (66 MHz on request) » 3.3 V or 5 V (universal PCI interface) » Support for up to seven peripheral slots (7x REQ/GNT signals) When installed in a peripheral slot, the CP3010-SA is isolated from the CompactPCI bus. It receives power from the backplane and supports rear I/O. CP3010-SA removal under power: When installed in a peripheral slot, the CP3010-SA supports hot plugging on the power interface through a dedicated power controller, but not on the PCI interface. Hot swapping of peripheral boards controlled by the CP3010-SA: When installed in the system slot, the CP3010-SA supports the hot swapping of other boards. Individual clocks for each slot and Enum signal handling are in compliance with the PICMG 2.1 Hot Swap Specification. The CP3010-SA itself, however, is not hot swappable. When installed in the system slot, the system must be powered down in order to replace the board.
	Rear I/O	The following interfaces are routed to the rear I/O connector J2: » COMA and COMB, or COMA and GPIO (all ports have 3.3V LVTTL signaling) » General purpose signals: 5 x GPIs and 3 x GPOs » 2 x USB 2.0 » 1 x CRT VGA » 2 x Gigabit Ethernet » 2 x SATA 3Gb/s » System management signals » Input for 5V standby power » System write protection

Table 1: CP3010-SA Main Specifications (Continued)

FEATURES		SPECIFICATIONS
Interfaces	DisplayPort	Two DisplayPort interfaces (DVI/HDMI-capable through passive cable adapter) for connection to monitors
	Gigabit Ethernet	Three 10 Base-T/100 Base-TX/1000 Base-T Gigabit Ethernet interfaces based on three Intel® I210-IT Ethernet controllers: » Two interfaces with Wake-on-LAN support and individually switchable to front I/O or rear I/O » One interface available on the high-speed I/O extension connector, J7, for the CP3010-HDD
	USB	Four USB ports: » One USB 3.0 port on the front I/O » One USB 2.0 port on the front I/O » Two USB 2.0 ports on the rear I/O CompactPCI interface, one of them switchable to the high-speed I/O extension connector, J7, for the CP3010-HDD
	Serial	Two 16C550-compatible UARTs: » COMA available either on the rear I/O or on the high-speed I/O extension connector, J7, for the CP3010-HDD » COMB or GPIO available on the rear I/O only
	SATA	Two SATA 3 Gb/s ports: » One SATA port either onboard for the SATA Flash or the CFast card, or on the rear I/O » One SATA port either on the rear I/O or on the high-speed I/O extension connector, J7, for the CP3010-HDD
	I/O Extension Interfaces	I/O extension to 8 HP board version via the CP3010-HDD extension module: » SATA 3 Gb/s for 2.5” HDD/SSD » USB 2.0 » Gigabit Ethernet » COMA » Audio Line In » Audio Line Out » CAN » Reset button » HDD/SSD activity LED
Sockets	Front Panel Connectors	» DP: two standard DisplayPort connectors, J3 and J6 » USB 3.0: one standard 9-pin, type A connector, J8 » USB 2.0: one standard 4-pin, type A connector, J9 » Ethernet: one standard dual RJ-45 connector, J10A/B
	Onboard Connectors	» CompactPCI connectors, J1 and J2 » CFast socket, J5 (optional) » 60-pin, high-speed I/O extension connector, J7, for connection to the CP3010-HDD extension module » JTAG connector, J4 » XDP-SFF (debug) connector, J12 » SPI extension connector, J11

Table 1: CP3010-SA Main Specifications (Continued)

FEATURES		SPECIFICATIONS
LEDs / Switches	Front Panel LEDs	System Status LEDs: » TH (red/green): Temperature Status » WD (green): Watchdog Status General Purpose LEDs: » LED3..0 (red/green/red+green): General Purpose / POST Code Ethernet LEDs: » ACT (green): Network / Link Activity » SPEED (green/orange): Network Speed
	DIP Switch	One DIP switch, SW1, for board configuration
Timer	Real Time Clock	Real-time clock with 242 Byte CMOS RAM; battery-backup available
	Watchdog Timer	Software-configurable, two-stage Watchdog with programmable timeout ranging from 125 ms to 4096 s in 16 steps Serves for generating IRQ or hardware reset
Sys. Management	Thermal Management	CPU and board overtemperature protection is provided by: » Up to four Digital Thermal Sensors (DTS), one for each core » One DTS for the Bus Interface Unit (BIU) within the SoC » Two DTS integrated in the SPD EEPROMs near to the DDR3L memory banks » Specially designed heat sinks
Security	TPM	Trusted Platform Module (TPM) 1.2 for enhanced hardware- and software-based data and system security
Software	uEFI BIOS	Phoenix SecureCore Tiano™ (SCT) BIOS firmware based on the uEFI Specification and the Intel Platform Innovation Framework for EFI: » LAN boot capability for diskless systems (standard PXE) » Redundant image; fail-safe recovery in case of a damaged image » Non-volatile storage of setting in the SPI boot flash (battery only required for the RTC) » Compatibility Support Module (CSM) providing legacy BIOS compatibility based on Phoenix SCT3 » Command shell for diagnostics and configuration » uEFI Shell commands executable from mass storage device in a pre-OS environment (open interface)
	Operating Systems	There are various operating systems available for the CP3010-SA. For further information, please contact Kontron.

Table 1: CP3010-SA Main Specifications (Continued)

FEATURES		SPECIFICATIONS
General	Power Consumption	See Chapter 4 for details.
	Temperature Range	Operational: 0°C to +60°C Standard (depending on the airflow in the system) -40°C to +85°C Extended (depending on the airflow in the system) Storage: -40°C to +85°C Without hard disk and without battery
	Battery	3.0V lithium battery for RTC; Battery type: UL-recognized CR2025 Temperature ranges: Operational (load): -20°C to +70°C typical (refer to the battery manufacturer's specifications for exact range) Storage (no load): -40°C to +70°C typical
	Climatic Humidity	93% RH at 40 °C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	100 mm x 160 mm 3U, 4 HP, CompactPCI-compliant form factor
	Board Weight	4 HP CP3010-SA with heat sink (without CFast card): 243 grams

Note: For information regarding the front panel of the 8 HP CP3010-SA with a CP3010-HDD extension module, refer to Chapter 6.

1.5 Standards

This product complies with the requirements of the following standards.

Table 2: Standards

TYPE	ASPECT	STANDARD	REMARKS
CE	Emission	EN 55011, EN 61000-6-4, EN 50155, EN 50121-3-2 (Class B)	
	Immunity	EN 50155, EN 61000-6-2, EN 50121-3-2	
	Electrical Safety	EN 60950-1	
Mechanical	Mechanical Dimensions	IEEE 1101.10	
Environmental	Climatic Humidity	IEC 60068-2-78 (see note below)	
	WEEE	Directive 2002/96/EC	Waste electrical and electronic equipment
	RoHS 2	Directive 2011/65/EU	Restriction of the use of certain hazardous substances in electrical and electronic equipment
	Operating Vibration	IEC 60068-2-6	Test parameters: 10-300 [Hz] frequency range 5 [g] acceleration 1 [oct/min] sweep rate 10 cycles/axis 3 directions
	Operating Shocks	IEC 60068-2-27	Test parameters: 30 [g] acceleration 12 [ms] shock duration half sine 3 shocks per direction (total: 18) 18 directions 5 [s] recovery time
	Operating Bumps	IEC 60068-2-27	Test parameters: 15 [g] acceleration 11 [ms] shock duration half sine 500 shocks per direction 6 directions 1 [s] recovery time

Note: Customers desiring to perform further environmental testing of the CP3010-SA must contact Kontron for assistance prior to performing any such testing.

Boards **without conformal coating** must not be exposed to a change of temperature which can lead to condensation. Condensation may cause irreversible damage, especially when the board is powered up again.

Kontron does not accept any responsibility for damage to products resulting from destructive environmental testing.

Furthermore, boards with extended temperature range comply with the following standards as well.

Table 3: Additional Standards for Boards with Extended Temperature Range

TYPE	ASPECT	STANDARD	REMARKS
Thermal	Operating Low Temperature Railway TX	IEC 60068-2-1 Test Ad: Cold	Test parameters: -40 [°C] ± 2 [°C] 16 [h] duration 1 cycle 1 [h] recovery (0.5 °C/min)
	Operating High Temperature Railway TX	IEC 60068-2-2 Test Bd: Dry Heat	Test parameters: +85[°C] ± 2[°C] 16 [h] duration 1 cycle
Environmental	Operating Vibration Railway Category 1, Class B	IEC 61000-2-64 Test Fh	Test parameters: 5-150 [Hz] frequency range ASD Spectrum [(m/s²)²/f] intensity of random vibration signal vs. frequency for X, Y, Z 1.00-0.45-0.70 [m/s²] rms max. 10 [min] duration for each direction X, Y, Z
	Operating Shocks Railway Category 1, Class B	IEC 60068-2-27	Test parameters: 30-30-50 [m/s²] acceleration x-y-z 30-30-50 [ms] recovery time x-y-z 3 shocks per direction (total: 18) 18 shocks

1.6 Related Publications

The following publications contain information relating to this product.

Table 4: Related Publications

PRODUCT	PUBLICATION
CompactPCI Systems	PICMG® 2.0, Rev. 3.0 CompactPCI® Specification
CFast	CFast Specification Revision 1.1
Platform Firmware	Unified Extensible Firmware Interface (uEFI) specification, version 2.3.1
All Kontron products	Product Safety and Implementation Guide, ID 1021-9142

2 Functional Description

2.1 Processor

The CP3010-SA supports the Intel® Atom™ E3845, and the Intel® Atom™ E3827 processors.

Table 5: Features of the Processors Supported on the CP3010-SA

FEATURE	Intel® Atom™ E3845, 1.91 GHz	Intel® Atom™ E3827, 1.75 GHz
Processor Cores	four	two
Processor Base Frequency	1.91 GHz	1.75 GHz
SpeedStep®	supported	supported
L1 cache per core	56 kB	56 kB
L2 cache	2 x 1 MB	2 x 512 kB
DDR3L Memory	up to 8 GB / 1333 MHz	up to 8 GB / 1333 MHz
Graphics Base Frequency	542 MHz	542 MHz
Graphics Max. Dynamic Frequency	792 MHz	792 MHz
Thermal Design Power	10 W	8 W

For further information about the processors used on the CP3010-SA, please visit the Intel website. For further information concerning the suitability of other Intel processors for use with the CP3010-SA, please contact Kontron.

2.1.1 Integrated Processor Graphics Controller

The Intel® Atom™ processor includes a highly integrated processor graphics controller delivering high-performance 3D, 2D graphics capabilities. The integrated processor graphics controller has two independent display pipes allowing for dual display configurations. It provides support for either two digital ports capable of driving resolutions up to 2560 x 1600 pixels @ 60 Hz through DisplayPort, or one VGA port and one digital port capable of driving resolutions up to 2560 x 1600 pixels @ 60 Hz.

2.2 Memory

The CP3010-SA supports a soldered, dual-channel (144-bit), Double Data Rate (DDR3L) memory without Error Checking and Correcting (ECC) running at 1333 MHz. The available memory configuration can be either 4 GB or 8 GB.

However, when the internal graphics controller is enabled, the amount of memory available to applications is less than the total physical memory in the system. The SoC dynamically allocates the proper amount of system memory required by the operating system and the application.

2.3 Watchdog Timer

The CP3010-SA provides a Watchdog timer that is programmable for a timeout period ranging from 125 ms to 4096 s in 16 steps.

The Watchdog timer provides the following modes or operation:

- Timer-only mode
- Reset mode
- Interrupt mode
- Dual-stage mode

In dual-stage mode, a combination of both interrupt and reset is generated if the Watchdog is not serviced.

2.4 Battery

The CP3010-SA is provided with an UL-recognized CR2025, 3.0 V, "coin cell" lithium battery for the RTC. Power for the RTC may be provided either from the 4 HP/8 HP CP3010-SA or from the backplane/rear transition module, i.e. only one battery may be used at a time in a system. When a battery is installed, refer to the operational specifications of the battery as this determines the storage temperature of the CP3010-SA.

2.5 Flash Memory

The CP3010-SA provides flash interfaces for the uEFI BIOS and the SATA flash.

2.5.1 SPI Boot Flash for uEFI BIOS

The CP3010-SA provides two 8 MB SPI boot flashes for two separate uEFI BIOS images, a standard SPI boot flash and a recovery SPI boot flash. The switching mechanism for the uEFI BIOS recovery is controlled via the DIP switch SW1, switch 2. The SPI boot flash includes a hardware write protection option, which can be configured via the uEFI BIOS. If write protection is enabled, the SPI boot flash cannot be written to.

Note: The uEFI BIOS code and settings are stored in the SPI boot flashes. Changes made to the uEFI BIOS settings are available only in the currently selected SPI boot flash. Thus, switching over to the other SPI boot flash may result in operation with different uEFI BIOS code and settings.

2.5.2 SATA Flash

For flexible flash extension, the CP3010-SA provides either a CFast socket, J5, for a SATA 3Gb/s CFast memory card, or up to 64 GB soldered SLC-based NAND flash memory with built-in full hard disk emulation, up to 60 MB/s read rate, and up to 55 MB/s write rate.

Note: Write protection is available for both the CFast card and the soldered NAND flash. Please contact Kontron for further assistance if write protection is required.

2.6 Trusted Platform Module 1.2

The CP3010-SA supports the Trusted Platform Module (TPM) 1.2. TPM1.2 is a security chip specifically designed to provide enhanced hardware- and software-based data and system security. TPM1.2 is based on the Atmel AT97SC3204 security controller and stores sensitive data such as encryption and signature keys, certificates and passwords, and is able to withstand software attacks to protect the stored information.

2.7 Board Interfaces

2.7.1 Front Panel LEDs

The CP3010-SA provides two system status LEDs, one temperature status LED (TH LED) and one Watchdog status LED (WD LED), as well as four General Purpose/POST code LEDs (LED3..0). Their functionality is described in the following chapters and reflected in the registers mentioned in Chapter 3, Configuration.

2.7.1.1 System Status LEDs

Table 6: System Status LEDs Function

LED	COLOR	STATE	FUNCTION
TH LED	red / green	Off	Power failure
		Green	Board in normal operation
		Red	CPU operating temperature has exceeded its defined operating limit
		Red blinks	CPU temperature above 110°C (CPU has been shut off) In this event, all General Purpose LEDs (LED3..0) are blinking red as well.
WD LED	red / green	OFF	Watchdog inactive
		Green	Watchdog active, waiting to be triggered
		Red	Watchdog expired

Note: If the TH LED flashes red at regular intervals, it indicates that the processor junction temperature has reached a level beyond which permanent silicon damage may occur and the processor has been shut off. To return to normal operation, the power must be switched off and then on again.

2.7.1.2 General Purpose LEDs

The General Purpose LEDs (LED3..0) are designed to indicate the boot-up POST code after which they are available to the application. If the LED3..0 are lit red during boot-up, a failure is indicated. In this event, please contact Kontron for further assistance.

The POST code is indicated during the boot-up phase. After boot-up, the LEDs indicate General Purpose or Port 80 signals, depending on the uEFI BIOS settings. The default setting after boot-up is General Purpose.

Table 7: General Purpose LEDs Function

LED	COLOR	FUNCTION DURING BOOT-UP	FUNCTION DURING uEFI BIOS POST (if POST code config. is enabled)	FUNCTION AFTER BOOT-UP
LED3	red	Power failure	--	General Purpose or Port 80 **Default: General Purpose**
	green	--	uEFI BIOS POST bit 3 and bit 7	
	red+green	--	--	
LED2	red	CPU catastrophic error	CPU catastrophic error	General Purpose or Port 80 **Default: General Purpose**
	green	--	uEFI BIOS POST bit 2 and bit 6	
	red+green	--	--	
LED1	red	Hardware reset	--	General Purpose or Port 80 **Default: General Purpose**
	green	--	uEFI BIOS POST bit 1 and bit 5	
	red+green	--	--	
LED0	red	uEFI BIOS boot failure	--	General Purpose or Port 80 **Default: General Purpose**
	green	--	uEFI BIOS POST bit 0 and bit 4	
	red+green	--	--	

For further information regarding the configuration of the General Purpose LEDs, refer to Chapter 3.3.7, LED Configuration Register, and Chapter 3.3.8, LED Control Register.

Note: The bit allocation for Port 80 is the same as for the POST code.

How to Read the 8-Bit POST Code

Due to the fact that only 4 LEDs are available and 8 bits must be displayed, the POST code output is multiplexed on the General Purpose LEDs.

Table 8: POST Code Sequence

STATE	GENERAL PURPOSE LEDs
0	All LEDs are OFF; start of POST sequence
1	High nibble
2	Low nibble; state 2 is followed by state 0

The following is an example of the General Purpose LEDs' operation if the POST configuration is enabled (see also Table 8, General Purpose LEDs Function).

Table 9: POST Code Example

	LED3	LED2	LED1	LED0	RESULT
HIGH NIBBLE	off (0)	on (1)	off (0)	off (0)	0x4
LOW NIBBLE	off (0)	off (0)	off (0)	on (1)	0x1
POST CODE	0x41				

Note: Under normal operating conditions, the General Purpose LEDs should not remain lit during boot-up. They are intended to be used only for debugging purposes. In the event that a General Purpose LED lights up during boot-up and the CP3010-SA does not boot, please contact Kontron for further assistance.

2.7.2 USB Interfaces

The CP3010-SA provides four USB ports:

- One USB 3.0 port on the front I/O
- One USB 2.0 port on the front I/O
- Two USB 2.0 ports on the rear I/O, one of them switchable to the high-speed I/O extension connector, J7, for the CP3010-HDD extension module

On the front panel, the CP3010-SA has one standard, type A, USB 3.0 connector, J8, and one standard, type A, USB 2.0 connector, J9.

2.7.3 DisplayPort Interfaces

The CP3010-SA provides two standard DisplayPort interfaces for connection to two monitors. The interfaces are implemented as standard DisplayPort connectors, J3 and J6, on the front panel.

2.7.4 Serial Ports

The CP3010-SA provides two serial ports:

- COMA available either on the CompactPCI rear I/O connector (3.3V LVTTL) or on the CP3010-HDD extension module
- COMB on the CompactPCI rear I/O connector (3.3V LVTTL)

COMA and COMB are fully compatible with the 16C550 controller and include a complete set of handshaking and modem control signals. The COMA and COMB ports provide maskable interrupt generation. The data transfer on the COM ports is up to 115.2 kbit/s.

2.7.5 Gigabit Ethernet

The CP3010-SA board includes three 10Base-T/100Base-TX/1000Base-T Ethernet ports based on three Intel® I210-IT Ethernet controllers (two onboard and one on the CP3010-HDD extension module). All three controllers are connected to the x1 PCI Express interfaces of the Intel® Atom™ processor. Two Gigabit Ethernet interfaces are individually switchable between front I/O and rear I/O and provide Wake-on-LAN support. One interface is available on the high-speed I/O extension connector, J7, for the CP3010-HDD module.

Note: In order to use the Wake-on-LAN feature, the power supply must not be switched off (+5V stand-by voltage cannot be used). The CP3010-SA does not turn off the main power supply after an operating system shutdown in order to support Wake-on-LAN.

Two of the Gigabit Ethernet interfaces are implemented as a standard RJ-45 Ethernet connectors, J10A/B on the front panel.

2.7.6 SATA Interfaces

The CP3010-SA provides two SATA ports:

- One SATA 3 Gb/s port either onboard for the SATA Flash or the CFast card, or on the CompactPCI rear I/O interface
- One SATA 3 Gb/s port either on the CompactPCI rear I/O interface or on the high-speed I/O extension connector, J7, for the CP3010-HDD extension modules

2.7.7 Debug Interface

The CP3010-SA provides several onboard options for hardware and software debugging, such as:

- Four bicolor general purpose LEDs (LED0..3), which indicate hardware failures, uEFI BIOS POST codes and user-configurable outputs
- One JTAG connector, J4, for programming the onboard logic
- One XDP-SFF, processor JTAG connector, J12, for facilitating the debug and uEFI BIOS software development

2.7.8 CompactPCI Interface

The CP3010-SA supports a flexible CompactPCI interface with a hot plug power interface (no PCI hot swap). In the system slot the PCI interface is in transparent mode, and in the peripheral slot the CompactPCI interface is isolated so that it cannot communicate with the CompactPCI bus. This mode is known as "passive mode".

2.7.8.1 Board Functionality when Installed in System Slot

In a system slot, the CompactPCI interface is provided as 32-bit/33 MHz (66 MHz on request) PCI interface. The CP3010-SA supports up to seven peripheral slots through a CompactPCI backplane.

Note: The CP3010-SA supports universal PCI V(I/O) signaling voltages with one common resistor configuration. For both 5V and 3.3 V PCI signaling voltages, 2.7 kΩ pull-up resistors are used.

2.7.8.2 Board Functionality when Installed in Peripheral Slot (Passive Mode)

In a peripheral slot, the board receives power but does not communicate on the CompactPCI bus; all CompactPCI signals are isolated.

2.7.8.3 Front / Rear I/O Configuration

The CP3010-SA is available in two versions:

- » CP3010-SA front I/O version
- » CP3010-SA rear I/O version

Please ensure that the correct version is stated on the order. If the CP3010-SA is ordered with rear I/O configuration, various I/O interfaces and signals are available via the CompactPCI connector J2, such as USB, SATA, GbE, VGA, and COM, as well as power and management signals. If the CP3010-SA is ordered with front I/O configuration, the I/O interfaces and signals mentioned above are isolated from the CompactPCI connector J2.

Note: The CP3010-SA with front I/O configuration does not provide a 64-bit termination to the backplane via the CompactPCI connector J2. This is different than on previous boards such as CP307 or CP308 where 64-bit termination is provided.

2.7.8.4 Board Insertion / Replacement under Power

The following features are implemented on the CP3010-SA:

- » Power ramping
- » ENUM signal handling (hot swapping of peripheral boards)

Power ramping on the CP3010-SA provides the hot plug functionality on the power interface. The PCI signal interface does not provide hot swap functionality. No microswitch, no blue LED and no signal precharge are provided on the CP3010-SA.

The ENUM signal on the CP3010-SA allows for hot swapping of peripheral boards with hot swap capability when the CP3010-SA is installed in the system slot.

Note: The CP3010-SA itself is not hot swappable when inserted in a system slot. When inserted in a peripheral slot, the CP3010-SA is hot pluggable.

2.7.8.5 Power Ramping

On the CP3010-SA a special power controller is used to ramp up the onboard supply voltages. This is done to avoid transients on the +3.3V and +5V power supplies from the system. When the power supply is stable, the power controller generates an onboard reset to put the board into a defined state.

2.7.8.6 ENUM# Interrupt

If the board is operated in the system slot, the ENUM signal is an input.

2.7.9 CompactPCI Connectors J1 and J2

The CP3010-SA provides two CompactPCI connectors, J1 and J2, with the following functionality:

- J1:32-bit CompactPCI interface with PCI bus signals, arbitration, clock and power
- J2: arbitration, clock and optionally rear I/O interface functionality

The CP3010-SA is designed for a CompactPCI bus architecture and the board is capable of driving up to seven CompactPCI slots with individual arbitration and clock signals.

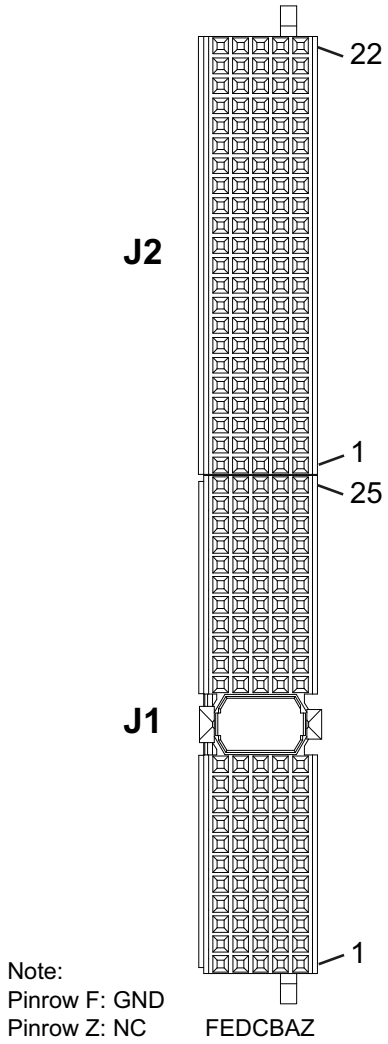
The CompactPCI standard is electrically identical to the PCI local bus. However, these systems are enhanced to operate in rugged industrial environments and to support multiple slots.

2.7.9.1 CompactPCI Connector Keying

CompactPCI backplane connectors support guide lugs to ensure a correct polarized mating (3.3 V or 5 V V(I/O) coding).

The CP3010-SA supports universal (3.3 V and 5 V) PCI V(I/O) signaling voltages with one common termination resistor configuration. Therefore, the CP3010-SA can be inserted in both, 3.3 V and 5 V CompactPCI systems and provides itself no guide lug.

Figure 5: CPCI Connectors J1/J2



2.7.9.2 CompactPCI Connectors J1 and J2 Pinouts

The CP3010-SA is provided with two 2 mm x 2 mm pitch female CompactPCI bus connectors, J1 and J2.

Table 10: CompactPCI Connector J1 System Slot Pinout

PIN	Z	A	B	C	D	E	F
25	NC	5V	REQ64#	ENUM#	3.3V	5V	GND
24	NC	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	NC	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	NC	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	NC	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	NC	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	NC	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	NC	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	NC	3.3V	RSV	RSV	GND	PERR#	GND
16	NC	DEVSEL#	PCIXCAP	V(I/O)	STOP#	LOCK#	GND
15	NC	3.3V	FRAME#	IRDY#	BDSEL#	TRDY#	GND
12-14	Key Area						
11	NC	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	NC	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	NC	C/BE[3]#	NC	AD[23]	GND	AD[22]	GND
8	NC	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	NC	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	NC	REQ0#	CPCI_PRESENT#	3.3V	CLK0	AD[31]	GND
5	NC	NC	NC	RST#	GND	GNT0#	GND
4	NC	NC	HEALTHY#	V(I/O)	RSV	RSV	GND
3	NC	INTA#	INTB#	INTC#	5V	INTD#	GND
2	NC	TCK	5V	TMS	NC	TDI	GND
1	NC	5V	NC	TRST#	NC	5V	GND

The legacy IDE interrupts INTP (CompactPCI specification pin D4) and INTS (CompactPCI specification pin E4) are not implemented on the CP3010-SA. Therefore, pins D4 and E4 are reserved.

The IPMB system management bus (CompactPCI specification pins A4, B17, C17) is not implemented on the CP3010-SA. Therefore, pin A4 is not connected and pins B17 and C17 are reserved.

For further information regarding the above-mentioned reserved pins, please contact Kontron.

Table 11: CompactPCI Connector J1 Peripheral Slot Pinout

PIN	Z	A	B	C	D	E	F
25	NC	5V	*	*	3.3V	5V	GND
24	NC	*	5V	V(I/O)	*	*	GND
23	NC	3.3V	*	*	5V	*	GND
22	NC	*	GND	3.3V	*	*	GND
21	NC	3.3V	*	*	*	*	GND
20	NC	*	GND	V(I/O)	*	*	GND
19	NC	3.3V	*	*	GND	*	GND
18	NC	*	GND	3.3V	*	*	GND
17	NC	3.3V	RSV	RSV	GND	*	GND
16	NC	*	*	V(I/O)	*	*	GND
15	NC	3.3V	*	*	BDSEL#	*	GND
14-12	Key Area						
11	NC	*	*	*	GND	*	GND
10	NC	*	GND	3.3V	*	*	GND
9	NC	*	NC	*	GND	*	GND
8	NC	*	GND	V(I/O)	*	*	GND
7	NC	*	*	*	GND	*	GND
6	NC	*	CPCI_PRESENT#	3.3V	*	*	GND
5	NC	NC	NC	RST#**	GND	*	GND
4	NC	NC	HEALTHY#	V(I/O)	RSV	RSV	GND
3	NC	*	*	*	5V	*	GND
2	NC	TCK	5V	TMS	NC	TDI	GND
1	NC	5V	NC	TRST#	NC	5V	GND

Note: A * indicates that the signal normally present at this pin is disconnected from the CompactPCI bus when the CP3010-SA is inserted in a peripheral slot.
** When the CP3010-SA is inserted in a peripheral slot, the function of the RST# signal can be enabled or disabled.

Table 12: CompactPCI Connector J2 Pinout (CP3010-SA Front I/O Vers.)

PIN	Z	A	B	C	D	E	F
22	NC	GA4	GA3	GA2	GA1	GA0	GND
21	NC	CLK6	GND	RSV	RSV	RSV	GND
20	NC	CLK5	GND	RSV	RSV	RSV	GND
19	NC	GND	GND	RSV	RSV	RSV	GND
18	NC	RSV	RSV	RSV	RSV	RSV	GND
17	NC	RSV	RSV	PRST#	REQ6#	GNT6#	GND
16	NC	RSV	RSV	DEG#	RSV	RSV	GND
15	NC	RSV	RSV	FAL#	REQ5#	GNT5#	GND
14	NC	RSV	RSV	RSV	RSV	RSV	GND
13	NC	RSV	RSV	RSV	RSV	RSV	GND
12	NC	RSV	RSV	RSV	RSV	RSV	GND
11	NC	RSV	RSV	RSV	RSV	RSV	GND
10	NC	RSV	RSV	RSV	RSV	RSV	GND
9	NC	RSV	GND	RSV	RSV	RSV	GND
8	NC	RSV	RSV	RSV	GND	RSV	GND
7	NC	RSV	RSV	RSV	RSV	RSV	GND
6	NC	RSV	RSV	RSV	GND	RSV	GND
5	NC	RSV	GND	RSV	RSV	RSV	GND
4	NC	V(I/O)	RSV	RSV	RSV	RSV	GND
3	NC	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	NC	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	NC	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

Note: The 64-bit CompactPCI signals are not used on the board and the 64-bit control and address signals are not terminated to V(I/O).

2.7.9.3 Optional Rear I/O Interface

The CP3010-SA board provides optional rear I/O connectivity for peripherals. When the rear I/O module is used, the signals of some of the main board / front panel connectors are routed to the rear I/O module interface.

The CP3010-SA with rear I/O is compatible with all standard 3U CompactPCI passive backplanes with rear I/O support.

Note: To support the rear I/O feature, a 3U CompactPCI backplane with rear I/O support is required. Do not plug a rear I/O configured board in a backplane without rear I/O support. Failure to comply with the above will result in damage to your board.

The CP3010-SA rear I/O provides the following interfaces (all signals are available on J2 only if the board is ordered with rear I/O functionality):

- Two USB 2.0 ports
- Two Gigabit Ethernet ports without LED signals
- Two SATA ports
- COMA and COMB, or COMA and GPIO (all ports have 3.3V LVTTL signaling)
- General purpose signals: 5 x GPIs and 3 x GPOs
- VGA analog port
- Management and control signals
- System write protection
- Input for +5V standby power
- Geographic addressing (GA[4..0])

Note: The pinout of the rear I/O CompactPCI connector on the CP3010-SA is compatible with that of the CP305, CP307, CP308, and CP3002. Thus, rear I/O modules designed for these boards can also be used with the CP3010-SA.

Table 13: Rear I/O CompactPCI Connector J2 Pinout (CP3010-SA Rear I/O Vers.)

PIN	Z	A	B	C	D	E	F
22	NC	GA4	GA3	GA2	GA1	GA0	GND
21	NC	CLK6	GND	USBA+	USBB+	USBA_PWR_5V	GND
20	NC	CLK5	GND	USBA-	USBB-	USBB_PWR_5V	GND
19	NC	GND	GND	PWR_BTN#	PWR_SLPS3#	RIO_3.3V	GND
18	NC	COMA_RXD	COMA_DCD#	COMA_DTR#	GPI1/ COMB_CTS#	COMA_CTS#	GND
17	NC	COMA_TXD	GPI0/ COMB_RXD	PRST#	REQ6#	GNT6#	GND
16	NC	COMA_DSR#	COMA_RTS#	DEG#	GND	COMA_RI#	GND
15	NC	PWR_5VSTDBY	RIO_SYS_WP#	FAL#	REQ5#	GNT5#	GND
14	NC	IPA_DA+	IPA_DA-	GPO1/ COMB_RTS#	IPA_DC+	IPA_DC-	GND
13	NC	IPA_DB+	IPA_DB-	GPI4/ COMB_RI#	IPA_DD+	IPA_DD-	GND
12	NC	IPB_DA+	IPB_DA-	RIO_1V9	IPB_DC+	IPB_DC-	GND
11	NC	IPB_DB+	IPB_DB-	GPI3/ COMB_DCD#	IPB_DD+	IPB_DD-	GND
10	NC	NC	GPO0/ COMB_TXD	VGA_RED	GPO2/ COMB_DTR#	NC	GND
9	NC	SATAATX+	GND	VGA_HSYNC	NC	SATABTX+	GND
8	NC	SATAATX-	NC	VGA_BLUE	GND	SATABTX-	GND
7	NC	NC	GPI2/ COMB_DSR#	VGA_DDC_DATA	RSV	NC	GND
6	NC	SATAARX+	NC	VGA_GREEN	GND	SATABRX+	GND
5	NC	SATAARX-	GND	VGA_VSYNC	NC	SATABRX-	GND
4	NC	VI/O	RIO_5V	VGA_DDC_CLK	GPIO_CFG0	NC	GND
3	NC	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	NC	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	NC	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

Note: The RIO_XXX signals are power supply **OUTPUTS** to supply the rear I/O module with power. These pins **MUST NOT** be connected to any other power source, either within the backplane itself or within a rear I/O module. Failure to comply with the above will result in damage to your board.

Table 14: CompactPCI Rear I/O Connector J3 Signals

SIGNAL	DESCRIPTION
COMAx	COMA port LVTTL (3.3V)
COMBx	COMB port LVTTL (3.3V)
GPI/GPO	General purpose input / general purpose output signal
GPIO_CFG0	GPIO or COMB configuration
IPx	Gigabit Ethernet copper port
SATAx	SATA port
USBx	USB interface and power

Table 14: CompactPCI Rear I/O Connector J3 Signals (Continued)

SIGNAL	DESCRIPTION
VGAx	VGA signal
RIOx/VI/O	Power supply signal
PWRx	Power management signal
RSV	Reserved
GND	Ground signal
NC	Not connected

With the GPIO_CFG0 signal on the rear I/O module an active COMB or GPIO interface can be selected.

Table 15: GPIO Signal Description

GPIO SIGNAL	DESCRIPTION
GPIO_CFG0	0 = GPIO 1 = COMB

Note: The default value is 1 if pin D4 is not connected (pull-up resistor to 3.3V on CP3010-SA). If the pin is connected, the default value depends on the rear I/O module. If the pin is driven by the rear I/O module, it must be considered that the CP3010-SA tolerates only 3.3 V signaling on this input.

2.7.9.4 Rear I/O Pin Description

Serial Ports

The CP3010-SA provides two serial ports, COMA and COMB, both available on the rear I/O CompactPCI connector J2.

Table 16: COMA and COMB Signal Description

PIN on J2	SIGNAL	FUNCTION	DRIVEN BY	SIGNALING VOLTAGE
A17	COMA_TXD	TXD serial port (COMA)	CP3010-SA	LVTTL (3.3V)
A18	COMA_RXD	RXD serial port (COMA)	Rear I/O module	LVTTL (3.3V)
E18	COMA_CTS#	CTS signal serial port (COMA)	Rear I/O module	LVTTL (3.3V)
B16	COMA_RTS#	RTS signal serial port (COMA)	CP3010-SA	LVTTL (3.3V)
A16	COMA_DSR#	DSR signal serial port (COMA)	Rear I/O module	LVTTL (3.3V)
B18	COMA_DCD#	DCD signal serial port (COMA)	Rear I/O module	LVTTL (3.3V)
C18	COMA_DTR#	DTR signal serial port (COMA)	CP3010-SA	LVTTL (3.3V)
E16	COMA_RI#	RI signal serial port (COMA)	Rear I/O module	LVTTL (3.3V)
B10	COMB_TXD	TXD serial port (COMB)	CP3010-SA	LVTTL (3.3V)
B17	COMB_RXD	RXD serial port (COMB)	Rear I/O module	LVTTL (3.3V)
D18	COMB_CTS#	CTS signal serial port (COMB)	Rear I/O module	LVTTL (3.3V)
C14	COMB_RTS#	RTS signal serial port (COMB)	CP3010-SA	LVTTL (3.3V)
B7	COMB_DSR#	DSR signal serial port (COMB)	Rear I/O module	LVTTL (3.3V)
C11	COMB_DCD#	DCD signal serial port (COMB)	Rear I/O module	LVTTL (3.3V)
D10	COMB_DTR#	DTR signal serial port (COMB)	CP3010-SA	LVTTL (3.3V)
C13	COMB_RI#	RI signal serial port (COMB)	Rear I/O module	LVTTL (3.3V)

Note: The pins for the interfaces COMA and COMB (pins A18, A17, A16, B18, B17, B16, B10, B7, C18, C14, C13, C11, D18, D10, E18, and E16) tolerate only 3.3V signaling and their inputs (driven by the rear I/O module) have internal pull-up resistors.

General Purpose Inputs/Outputs

Alternatively, the following GPIO signals are available instead of the COMB signals if pin D4 on the rear I/O connector J2 (GPIO_CFG0) is set to 0.

Table 17: GPIO Signal Description

PIN on J2	SIGNAL	FUNCTION	DRIVEN BY	SIGNALING VOLTAGE
B10	GPO0	General purpose output 0	CP3010-SA	LVTTL (3.3V)
B17	GPI0	General purpose input 0	Rear I/O module	LVTTL (3.3V)
D18	GPI1	General purpose input 1	Rear I/O module	LVTTL (3.3V)
C14	GPO1	General purpose output 1	CP3010-SA	LVTTL (3.3V)
B7	GPI2	General purpose input 2	Rear I/O module	LVTTL (3.3V)
C11	GPI3	General purpose input 3	Rear I/O module	LVTTL (3.3V)
D10	GPO2	General purpose output 2	CP3010-SA	LVTTL (3.3V)
C13	GPI4	General purpose input 4	Rear I/O module	LVTTL (3.3V)

Note: The pins for the GPIO interface (pins B17, B10, B7, C14, C13, C11, D18, and D10) tolerate only 3.3 V signaling and their inputs (driven by the rear I/O module) have internal pull-up resistors.

VGA Interface

VGA signals are available either on the front VGA connector, J6, or on the rear I/O interface due to the implemented switch on the CP3010-SA. Switching over from front to rear I/O or vice versa is effected using the uEFI BIOS.

Table 18: VGA Signal Description

PIN on J2	SIGNAL	FUNCTION	DRIVEN BY	SIGNALING VOLTAGE
C10	VGA_RED	VGA analog red signal	CP3010-SA	Analog
C6	VGA_GREEN	VGA analog green signal	CP3010-SA	Analog
C8	VGA_BLUE	VGA analog blue signal	CP3010-SA	Analog
C9	VGA_HSYNC	VGA horizontal synchronization signal	CP3010-SA	LVTTL (3.3 V)
C5	VGA_VSYNC	VGA vertical synchronization signal	CP3010-SA	LVTTL (3.3 V)
C4	VGA_DDC_CLK	Monitor control clock signal	CP3010-SA	TTL (5 V)
C7	VGA_DDC_DATA	Monitor control data signal	Bidirectional	TTL (5 V)

Note: On the rear I/O, the CP3010-SA provides 150 Ω termination resistors for the red, green and blue VGA signals. Thus, further 150 Ω termination resistors are necessary on the rear I/O module to reach the required 75 Ω termination for the VGA connection.

Ethernet Interfaces

Gigabit Ethernet signals are available either on the front RJ-45 connector or on the rear I/O interface due to the implemented switches on the CP3010-SA. Both Gigabit Ethernet channels are individually switchable to front or rear I/O. Switching over from front to rear I/O or vice versa is effected using the uEFI BIOS settings (default: front I/O).

Table 19: Gigabit Ethernet Signal Description

PIN on J2	SIGNAL	FUNCTION	DRIVEN BY	SIGNALING VOLTAGE
A14	IPA_DA+	Media-dependent interface port A	Bidirectional	Analog
B14	IPA_DA-	Media-dependent interface port A	Bidirectional	Analog
A13	IPA_DB+	Media-dependent interface port A	Bidirectional	Analog
B13	IPA_DB-	Media-dependent interface port A	Bidirectional	Analog
D14	IPA_DC+	Media-dependent interface port A	Bidirectional	Analog
E14	IPA_DC-	Media-dependent interface port A	Bidirectional	Analog
D13	IPA_DD+	Media-dependent interface port A	Bidirectional	Analog
E13	IPA_DD-	Media-dependent interface port A	Bidirectional	Analog
A12	IPB_DA+	Media-dependent interface port B	Bidirectional	Analog
B12	IPB_DA-	Media-dependent interface port B	Bidirectional	Analog
A11	IPB_DB+	Media-dependent interface port B	Bidirectional	Analog
B11	IPB_DB-	Media-dependent interface port B	Bidirectional	Analog
D12	IPB_DC+	Media-dependent interface port B	Bidirectional	Analog
E12	IPB_DC-	Media-dependent interface port B	Bidirectional	Analog
D11	IPB_DD+	Media-dependent interface port B	Bidirectional	Analog
E11	IPB_DD-	Media-dependent interface port B	Bidirectional	Analog
C12	RIO_1V9	Power supply for magnetics center tap	CP3010-SA	1.9V

Note: The Ethernet magnetics must be placed on the rear I/O module. The Ethernet magnetics center tap must be connected to the dedicated 1.9 V power supply provided by the CP3010-SA (pin C12 on J2).

Note: Pin C12 is a power supply **OUTPUT**. This pin **MUST NOT** be connected to any other power source, either within the backplane itself or within a rear I/O module. Failure to comply with the above will result in damage to your board.

SATA Interfaces

The CP3010-SA provides two SATA interfaces on the rear I/O CompactPCI connector J2.

Table 20: SATA Signal Description

PIN on J2	SIGNAL	FUNCTION	DRIVEN BY	SIGNALING VOLTAGE
A6	SATAARX+	Positive input port A	Rear I/O module	Differential
A5	SATAARX-	Negative input port A	Rear I/O module	Differential
A9	SATAATX+	Positive output port A	CP3010-SA	Differential
A8	SATAATX-	Negative output port A	CP3010-SA	Differential
E6	SATABRX+	Positive input port B	Rear I/O module	Differential
E5	SATABRX-	Negative input port B	Rear I/O module	Differential
E9	SATABTX+	Positive output port B	CP3010-SA	Differential
E8	SATABTX-	Negative output port B	CP3010-SA	Differential
B15	RIO_SYS_WP#	System write protection	CP3010-SA	LVTTL (3.3V)

USB Interfaces

Two USB 2.0 ports are available on the rear I/O CompactPCI connector J2.

Table 21: USB Signal Description

PIN on J2	SIGNAL	FUNCTION	DRIVEN BY	SIGNALING VOLTAGE
C21	USBA+	Positive USB port A	Bidirectional	Differential
C20	USBA-	Negative USB port A	Bidirectional	Differential
E21	USBA_PWR_5V	USB power supply 5 V port A	CP3010-SA	5 V
D21	USBB+	Positive USB port B	Bidirectional	Differential
D20	USBB-	Negative USB port B	Bidirectional	Differential
E20	USBB_PWR_5V	USB power supply 5 V port B	CP3010-SA	5 V

Power Supply and Power Management Signals

The CP3010-SA provides the following power supply and power management signals to the rear I/O module.

Table 22: Power Supply and Power Management Signal Description

PIN on J2	SIGNAL	FUNCTION	DRIVEN BY	SIGNALING VOLTAGE
B4	RIO_5V	Power supply 5 V	CP3010-SA	5 V
E19	RIO_3.3V	Power supply 3.3 V	CP3010-SA	3.3 V
A4	VI/O	Power supply VI/O	Backplane	5 V or 3.3 V
A15	PWR_5V_STDBY	Power supply 5 V standby	Rear I/O module	5 V
C19	PWR_BTN#	Power button signal	Rear I/O module	Open drain (pull-up resistor on the CP3010-SA) or LVTTL (3.3 V)
D19	PWR_SLPS3#	Sleep S3 signal	CP3010-SA	LVTTL (3.3 V)
D7	RSV	Reserved	--	--

Note: Pin D7 **MUST NOT** be connected to any signal, either within the backplane itself or within a rear I/O module. Failure to comply with the above will result in damage to your board.

Note: Pins B4 and E19 are power supply **OUTPUTS** to supply the rear I/O module with power. These pins **MUST NOT** be connected to any other power source, either within the backplane itself or within a rear I/O module. Failure to comply with the above will result in damage to your board.

For further information regarding the rear I/O signals, please contact Kontron.

3 Configuration

3.1 DIP Switch Configuration

The DIP switch SW1 provides the following switches for board configuration: POST code indication, SPI boot flash selection, system write protection configuration and uEFI BIOS configuration.

Figure 6: DIP Switch SW1

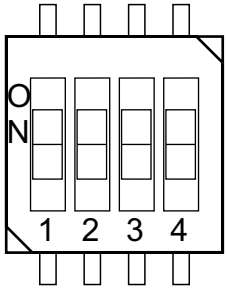


Table 23: DIP Switch SW1 Functionality

SWITCH	SETTING	FUNCTIONALITY
1	***OFF***	***Boot-up with POST code indication on LED3..0***
	ON	Boot-up with no POST code indication on LED3..0
2	***OFF***	***Boot from the standard SPI boot flash***
	ON	Boot from the recovery SPI boot flash
3	***OFF***	***Non-volatile memory write protection disabled*** (if no other write protection sources are enabled)
	ON	Non-volatile memory write protection enabled
4	***OFF***	***Boot using the currently saved uEFI BIOS settings***
	ON	Clear the uEFI BIOS settings and use the default values

The default setting is indicated by using italic bold.

To clear the uEFI BIOS settings and the passwords, proceed as follows:

1. Set DIP switch SW1, switch 4, to the ON position.
2. Apply power to the system.
3. Wait 30 seconds and then remove power from the system. During this time period no messages are displayed.
4. Set DIP switch SW1, switch 4, to the OFF position.

3.2 System Write Protection

The CP3010-SA provides write protection for non-volatile memories via the DIP switch SW1, the uEFI Shell and a backplane pin. If one of these sources is enabled, the system is write protected. Please contact Kontron for further information before using these functions.

3.3 CP3010-SA-Specific Registers

Table 24: CP3010-SA-Specific Registers

ADDRESS	DEVICE
0x284	Write Protection Register (WPROT)
0x285	Reset Status Register (RSTAT)
0x288	Board ID High-Byte Register (BIDH)
0x28A	Geographic Addressing Register (GEOAD)
0x28C	Watchdog Timer Control Register (WTIM)
0x28D	Board ID Low-Byte Register (BIDL)
0x290	LED Configuration Register (LCFG)
0x291	LED Control Register (LCTRL)
0x292	General Purpose Output Register (GPOUT)
0x293	General Purpose Input Register (GPIN)

3.3.1 Write Protection Register (WPROT)

The Write Protection Register holds the write protect signals for non-volatile devices.

Table 25: Write Protection Register (WPROT)

ADDRESS		0x284						
BIT	7	6	5	4	3	2	1	0
NAME	SWP	Reserved			SFWP	DSWP	BSWP	SSWP
ACCESS	R	R			R/W	R	R	R/W
RESET	0	000			0	0	0	0
BITFIELD		DESCRIPTION						
7	SWP	System write protection status: 0 = Onboard non-volatile memory devices not write protected 1 = Onboard non-volatile memory devices write protected						
3	SFWP	SATA Flash write protection status: 0 = SATA Flash / CFast memory not included in system write protection 1 = SATA Flash / CFast memory included in system write protection If this bit is programmed once, it cannot be reprogrammed.						
2	DSWP	This bit reflects the state of the system write protection via DIP switch SW1, switch 3: 0 = System not write protected via DIP switch 1 = System write protected						
1	BSWP	This bit reflects the state of the system write protection via backplane (SYS_WP#): 0 = System not write protected via backplane 1 = System write protected						
0	SSWP	This bit reflects the state of the system write protection via software: 0 = System devices not write protected via software 1 = System write protected If this bit is programmed once, it cannot be reprogrammed.						

3.3.2 Reset Status Register (RSTAT)

The Reset Status Register is used to determine the host's reset source.

Table 26: Reset Status Register (RSTAT)

ADDRESS	0x285							
BIT	7	6	5	4	3	2	1	0
NAME	PORS	Reserved				FPRS	CPRS	WTRS
ACCESS	R/W	R				R/W	R/W	R/W
RESET	N/A	0000				0	0	0

BITFIELD		DESCRIPTION
7	PORS	Power-on reset status: 0 = System reset generated by warm reset 1 = System reset generated by power-on (cold) reset Writing a '1' to this bit clears the bit.
2	FPRS	Front panel push button reset status: 0 = System reset not generated by front panel reset 1 = System reset generated by front panel reset Writing a '1' to this bit clears the bit.
1	CPRS	CompactPCI reset status (PRST signal): 0 = System reset not generated by CompactPCI reset input 1 = System reset generated by CompactPCI reset input Writing a '1' to this bit clears the bit.
0	WTRS	Watchdog timer reset status: 0 = System reset not generated by Watchdog timer 1 = System reset generated by Watchdog timer Writing a '1' to this bit clears the bit.

Note: The Reset Status Register is set to default values by power-on (cold) reset, not by a warm reset.

3.3.3 Board ID High-Byte Register (BIDH)

Table 27: Board ID High-Byte Register (BIDH)

ADDRESS	0x288							
BIT	7	6	5	4	3	2	1	0
NAME	BIDH							
ACCESS	R							
RESET	0xEF							
BITFIELD		DESCRIPTION						
7	BIDH	Board identification: CP3010-SA: 0xEF40						

3.3.4 Geographic Addressing Register (GEOAD)

The Geographic Addressing Register holds the CompactPCI geographic address (site number) used to assign the Intelligent Platform Management Bus (IPMB) address to the CP3010-SA.

Table 28: Geographic Addressing Register (GEOAD)

ADDRESS	0x28A							
BIT	7	6	5	4	3	2	1	0
NAME	Reserved			GA				
ACCESS	R			R				
RESET	000			N/A				
BITFIELD		DESCRIPTION						
7..5	Res.	Reserved						
4..0	GA	Geographic address						

Note: The Geographic Addressing Register is set to default values by power-on (cold) reset, not by a warm reset.

3.3.5 Watchdog Timer Control Register (WTIM)

Table 29: Watchdog Timer Control Register (WTIM)

ADDRESS	0x28C							
BIT	7	6	5	4	3	2	1	0
NAME	WTE	WMD		WEN/WTR	WTM			
ACCESS	R/W	R/W		R/W	R/W			
RESET	0	00		0	0000			

BITFIELD		DESCRIPTION
7	WTE	Watchdog timer expired status bit: 0 = Watchdog timer has not expired 1 = Watchdog timer has expired. Writing a '1' to this bit resets it to 0.
6..5	WMD	Watchdog mode: 00 = Timer only mode 01 = Reset mode 10 = Interrupt mode 11 = Cascaded mode (dual-stage mode)
4	WEN/WTR	Watchdog enable / Watchdog trigger control bit: 0 = Watchdog timer not enabled Prior to the Watchdog being enabled, this bit is known as WEN. After the Watchdog is enabled, it is known as WTR. Once the Watchdog timer has been enabled, this bit cannot be reset to 0. As long as the Watchdog timer is enabled, it will indicate a '1'. 1 = Watchdog timer enabled Writing a '1' to this bit causes the Watchdog to be retriggered to the timer value indicated by bits WTM[3..0].
3..0	WTM	Watchdog timeout settings: 0000 = 0.125 s 0001 = 0.25 s 0010 = 0.5 s 0011 = 1 s 0100 = 2 s 0101 = 4 s 0110 = 8 s 0111 = 16 s 1000 = 32 s 1001 = 64 s 1010 = 128 s 1011 = 256 s 1100 = 512 s 1101 = 1024 s 1110 = 2048 s 1111 = 4096 s

3.3.6 Board ID Low-Byte Register (BIDL)

Table 30: Board ID Low-Byte Register (BIDL)

ADDRESS	0x28D							
BIT	7	6	5	4	3	2	1	0
NAME	BIDL							
ACCESS	R							
RESET	0x40							
BITFIELD		DESCRIPTION						
7	BIDL	Board identification: CP3010-SA: 0xEF40						

3.3.7 LED Configuration Register (LCFG)

The LED Configuration Register holds a series of bits defining the onboard configuration for the front panel General Purpose LEDs.

Table 31: LED Configuration Register (LCFG)

ADDRESS	0x290							
BIT	7	6	5	4	3	2	1	0
NAME	Reserved				LCON			
ACCESS	R				R/W			
RESET	0000				0000			
BITFIELD		DESCRIPTION						
3..0	LCON	LED3..0 configuration: 0000 = POST Mode (LEDs build a binary vector to display Port 80 signals) 0001 = General Purpose Mode (LEDs are controlled via the LCTRL register) 0010 - 1111 = Reserved						

Beside the configurable functions described above, LED3..0 fulfill also a basic debug function during the power-up phase as long as the first access to Port 80 is processed. For further information on reading the 8-bit uEFI BIOS POST Code, refer to Chapter 2.7.1.2, General Purpose LEDs.

3.3.8 LED Control Register (LCTRL)

The LED Control Register enables the user to switch on and off the front panel General Purpose LEDs.

Table 32: LED Control Register (LCTRL)

ADDRESS	0x291							
BIT	7	6	5	4	3	2	1	0
NAME	LCMD				LCOL			
ACCESS	R/W				R/W			
RESET	0000				0000			

BITFIELD		DESCRIPTION
7..4	LCMD	LED command: 0000 = Get LED0 0001 = Get LED1 0010 = Get LED2 0011 = Get LED3 0100 - 0111 = Reserved 1000 = Set LED0 1001 = Set LED1 1010 = Set LED2 1011 = Set LED3 1100 - 1111 = Reserved
3..0	LCOL	LED color: 0000 = Off 0001 = Green 0010 = Red 0011 = Red+Green 0100 - 1111 = Reserved

Note: The LED Control Register can only be used if the General Purpose LEDs indicated in the “LED Configuration Register” (see Table 32) are configured in General Purpose Mode.

3.3.9 General Purpose Output Register (GPOUT)

The General Purpose Output Register holds the general purpose output signals of the rear I/O CompactPCI connector J2. This register can only be used if the CP3010-SA is ordered as a rear I/O version and the rear I/O GPIO operation is configured through the dedicated rear transition module configuration signal on the CompactPCI connector J2.

Table 33: General Purpose Output Register (GPOUT)

ADDRESS	0x292							
BIT	7	6	5	4	3	2	1	0
NAME	Reserved					GPO2	GPO1	GPO0
ACCESS	R					R/W	R/W	R/W
RESET	00000					0	0	0

BITFIELD		DESCRIPTION
2..0	GPO2..0	General purpose output signals (3.3V LVTTL): 0 = Output low 1 = Output high

3.3.10 General Purpose Input Register (GPIN)

The General Purpose Input Register holds the general purpose input signals of the rear I/O CompactPCI connector J2. This register can only be used if the CP3010-SA is ordered as a rear I/O version and the rear I/O GPIO operation is configured through the dedicated rear transition module configuration signal on the CompactPCI connector J2.

Table 34: General Purpose Input Register (GPIN)

ADDRESS	0x293							
BIT	7	6	5	4	3	2	1	0
NAME	Reserved			GPI4	GPI3	GPI2	GPI1	GPI0
ACCESS	R			R	R	R	R	R
RESET	000			1	1	1	1	1

BITFIELD		DESCRIPTION
4..0	GPI4.. 0	General purpose input signals (3.3V LVTTL): 0 = Input low 1 = Input high

Note: The CP3010-SA provides pull-up resistors on the rear I/O signal pins GPI[4..0], which leads to the default setting “input high” if the inputs are not connected.
The general purpose inputs support 3.3V LVTTL signaling only (not 5V-friendly).

4 Power Considerations

4.1 CP3010-SA Voltage Ranges

The CP3010-SA has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The system power supply must comply with the CompactPCI® specification.

The following table specifies the ranges for the input power voltage within which the board is functional.

Table 35: DC Operational Input Voltage Range

INPUT SUPPLY VOLTAGE	OPERATING RANGE
+3.3 V	3.2 V min. to 3.47 V max.
+5 V	4.85 V min. to 5.25 V max.
+5 V STDBY (optional)	4.85 V min. to 5.25 V max.

Note: Failure to comply with the instructions above may result in damage to the board or improper operation.

4.2 Power Consumption

The goal of this description is to provide a method to calculate the power consumption for the CP3010-SA baseboard and for additional configurations. The processor and the memory dissipate the majority of the thermal power.

The power consumption measurements were carried out using the following testing parameters:

- CP3010-SA installed in the system slot
- Ethernet ports not connected
- 4 GB DDR3 SDRAM in dual-channel mode
- +3.3V and +5V supply voltage
- 2.5 m/s airflow

The operating systems used were uEFI Shell and Windows® 8.1, 64-bit. All measurements were conducted at an ambient temperature of 25 °C. The power consumption values indicated in the tables below can vary depending on the ambient temperature. This can result in deviations of the power consumption values of up to 15%.

The power consumption was measured using the following the processors:

- Quad-core Intel® Atom™ E3845, 1.91 GHz, 2 MB L2 cache
- Dual-core Intel® Atom™ E3827, 1.75 GHz, 1 MB L2 cache

The power consumption was measured using the following configurations:

» Work load: uEFI Shell

For this measurement the processor cores were active, the graphics controller was in idle state (no application running).

» Work load: Idle

For this measurement all processor cores and the graphics controller were in idle state (no application running).

» Work load: Typical

For this measurement all processor cores were operating at maximum work load and the graphics controller was performing basic operation (e.g. dual-screen output configuration with no 3D graphics application running). These values represent the power dissipation reached under realistic, OS-controlled applications with the processor operating at maximum performance.

» Work load: Maximum

These values represent the maximum power dissipation achieved through the use of specific tools to heat up the processor cores and graphics controller. These values are unlikely to be reached in real applications.

Table 36: CP3010-SA Power Consumption

WORK LOAD	Intel® Atom™ E3845 1.91 GHz	Intel® Atom™ E3827 1.75 GHz
uEFI Shell	6.3 W	6.3 W
Idle	7.8 W	7.8 W
Typical	9.4 W	8.6 W
Maximum	14.3 W	11.6 W

The following table indicates the power consumption of the CP3010-SA accessories.

Table 37: Power Consumption of CP3010-SA Accessories

MODULE	POWER CONSUMPTION
SATA Flash module	approx. 1.0 W
Gigabit Ethernet (per interface)	approx. 0.5 W

5 Thermal Considerations

The thermal characteristic graphs shown in the following sections are intended to serve as guidance for reconciling the required computing power with the necessary system volumetric airflow over the ambient temperature. The graphs contain two curves representing upper level working points based on different levels of average CPU utilization. When operating below the corresponding curve, the CPU runs without any intervention of thermal supervision (the CPU is below 105°C). When operated above the corresponding curve, various thermal protection mechanisms may take effect resulting in temporarily reduced CPU performance or finally in an emergency stop (the CPU is at 110°C) in order to protect the CPU from thermal destruction (in this case the power must be switched off and then on again). In real applications this means that the board can be operated temporarily at a higher ambient temperature or at a reduced flow rate and still provide some margin for temporarily requested peak performance before thermal protection will be activated.

An airflow of 2.0 m/s to 3.0 m/s is a typical value for a standard *Kontron* ASM rack. For other racks or housings the available airflow will differ. The maximum ambient operating temperature must be determined for such environments.

How to read the diagram

Select a specific CPU and choose a specific working point. For a given flow rate there is a maximum airflow input temperature (= ambient temperature) provided. Below this operating point, thermal supervision will not be activated. Above this operating point, thermal supervision will become active protecting the CPU from thermal destruction. The minimum airflow rate provided must be more than the value specified in the diagram.

Volumetric flow rate

The volumetric flow rate refers to an airflow through a fixed cross-sectional area (i.e. slot width x depth. The volumetric flow rate is specified in m^3/h (cubic-meter-per-hour) or cfm (cubic-feet-per-minute) respectively.

Conversion: 1 cfm = 1.7 m^3/h; 1 m^3/h = 0.59 cfm

Airflow

At a given cross-sectional area and a required flow rate, an average, homogeneous airflow speed can be calculated using the following formula:

Airflow = Volumetric flow rate / area.

The airflow is specified in m/s (meter-per-second) or in fps (feet-per-second) respectively.

Conversion: 1 fps = 0.3048 m/s; 1 m/s = 3.28 fps

The following figures illustrate the thermal operational limits of the CP3010-SA taking into consideration power consumption vs. ambient air temperature vs. airflow rate.

Note: The CP3010-SA must be operated within the thermal operational limits indicated below.

5.1 Operational Limits for the CP3010-SA

Figure 7: CP3010-SA with Intel® Atom™ E3845, 1.91 GHz

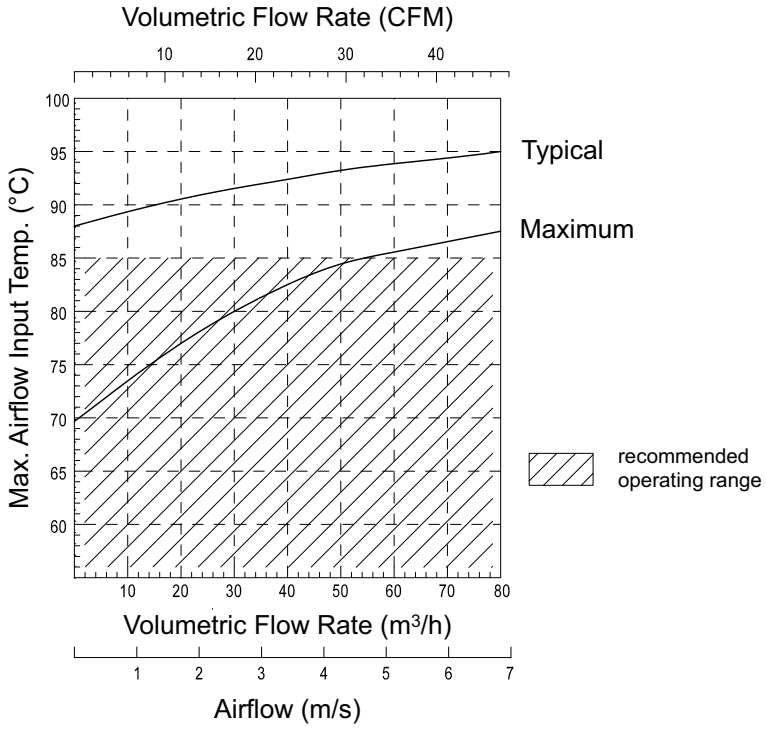
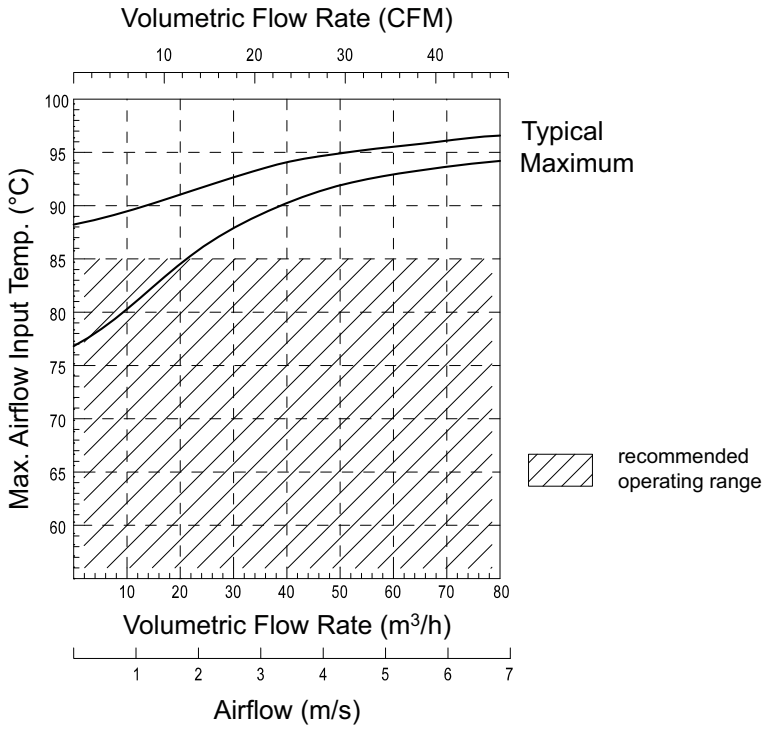


Figure 8: CP3010-SA with Intel® Atom™ E3827, 1.75 GHz



6 CP3010-HDD Extension Module

6.1 Overview

The CP3010-HDD is a factory-installed mezzanine extension module which along with an 8 HP front panel provides additional interfaces, such as:

- One CAN port (D-Sub connector)
- One COM port (RJ-45 connector)
- One USB 2.0 port
- One Gigabit Ethernet port
- Two audio ports (Line-In and Line-Out)
- One Reset switch
- One SATA activity LED
- One onboard SATA HDD/SSD interface
- Battery socket

Note: If a CP3010-HDD module is used on the CP3010-SA, either the CP3010-SA or the CP3010-HDD module may be equipped with a battery.
Using one battery on the CP3010-SA and one on the CP3010-HDD module simultaneously may result in premature discharge of the batteries.

6.2 Technical Specifications

Table 38: CP3010-HDD Module Specifications

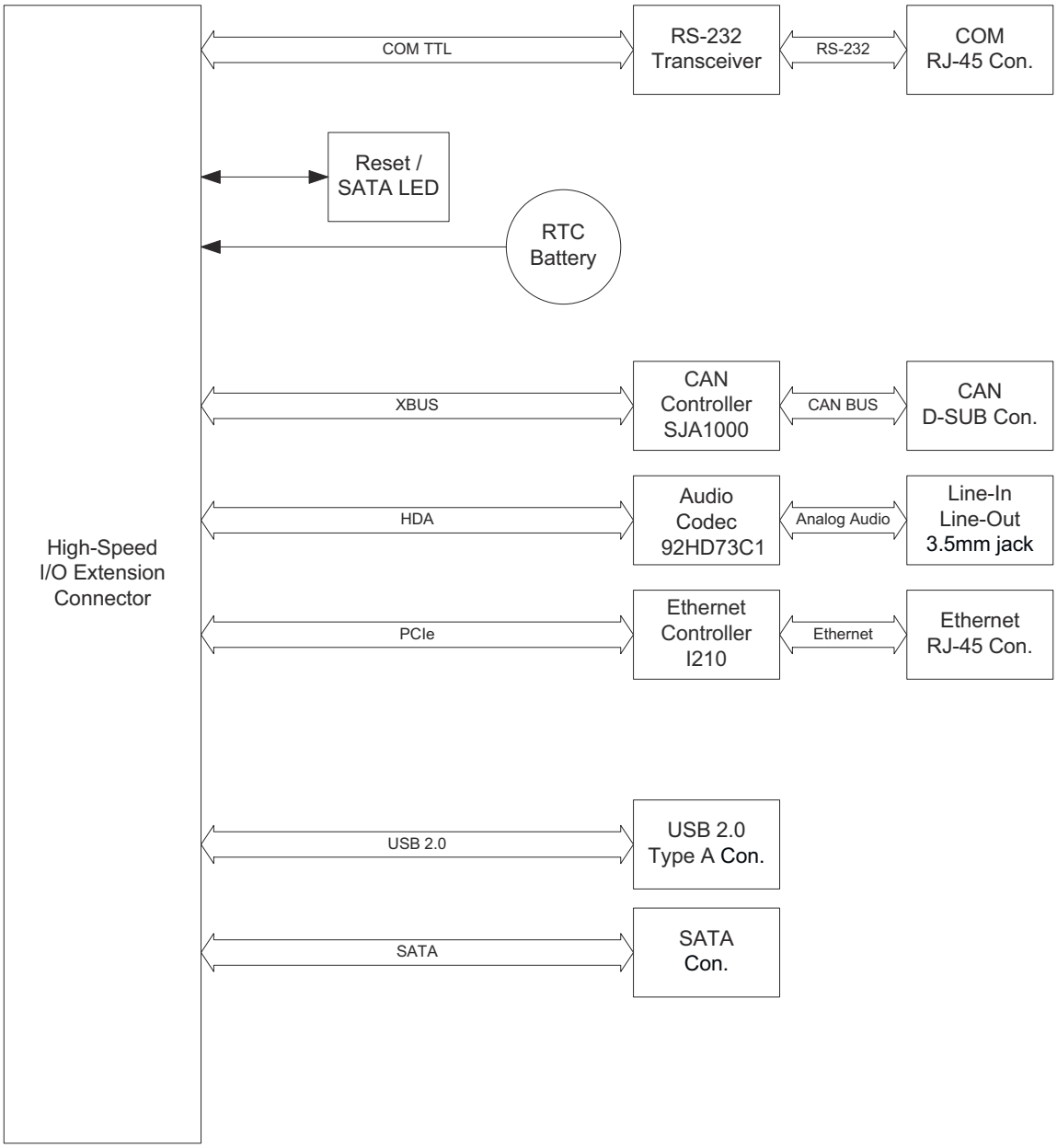
FEATURES		SPECIFICATIONS
Front Panel Interfaces	CAN	One standard 9-pin, D-Sub connector, J6
	Serial Port	One 16C550-compatible serial port, COMA (RS-232) RJ-45 connector, J3
	Gigabit Ethernet	One 10 Base-T/100 Base-TX/1000 Base-T Gigabit Ethernet interface based on one Intel® I210-IT Ethernet controller: » One standard RJ-45 connector, J2 (GbE C) » Wake-on-LAN support
	USB	One standard USB 2.0, type A connector, J1

Table 38: CP3010-HDD Module Specifications (Continued)

FEATURES		SPECIFICATIONS
Front Panel Interfaces	HD Audio	Line In: (Stereo) Sampling Rates: 8 kHz, 11.025 kHz, 16 kHz, 22.05 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, 192 kHz Dynamic Range: 85 dB ADC Resolution: 24-bit Input Impedance: 50 Ω, 15 pf Input Sensitivity: typ. 1 Vrms Total Harmonic Distortion (THD + N): -70 dB (0.032%) Connector: standard 3.5 mm stereo audio jack, J4 Line Out: (Stereo) Sampling Rates: 8 kHz, 11.025 kHz, 16 kHz, 22.05 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, 192 kHz Dynamic Range: 90 dB DAC Resolution: 24-bit Output Impedance: typ. 150 Ω External Load Impedance: min. 10 kΩ Total Harmonic Distortion (THD + N): -70 dB (0.032%) Connector: standard 3.5 mm stereo audio jack, J5
LEDs/ Switches	HDD LED (front panel)	One HDD LED (green) indicating HDD/SSD activity
	Switch (front panel)	Reset switch, guarded
General	Power Consumption	Power consumption without HDD/SSD or peripheral devices connected: approx. 1.0 W
	Temperature Range	Operational: 0°C to +60°C Standard -40°C to +85°C Extended Storage: -40°C to +85°C Without battery Note: When a battery is installed, refer to the operational specifications of the battery as this determines the storage temperature of the CP3010-HDD module (see "Battery" below).
	Battery	3.0V lithium battery for RTC; Battery type: UL-recognized CR2025 Temperature ranges: Operational (load): -20°C to +70°C typical (refer to the battery manufacturer's specifications for exact range) Storage (no load): -40°C to +70°C typical
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	CP3010-HDD: 100 mm x 160 mm CP3010-SA with CP3010-HDD: 3U, 8 HP, CompactPCI-compliant form factor
	Board Weight	CP3010-HDD: 150 grams (without HDD/SSD) 8HP CP3010-SA with CP3010-HDD: with heat sink (without HDD/SSD): 415 grams

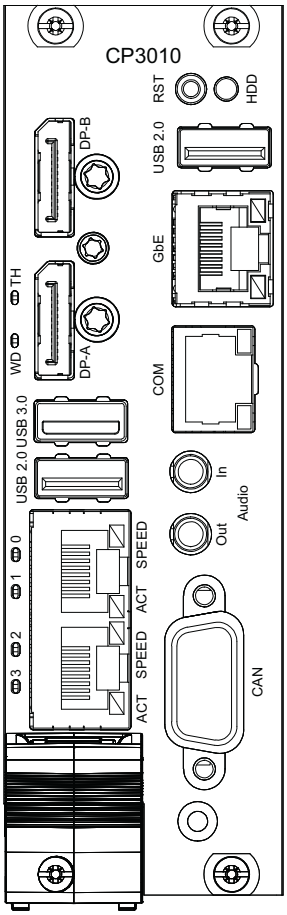
6.3 CP3010-HDD Module Functional Block Diagram

Figure 9: CP3010-HDD Module Functional Block Diagram



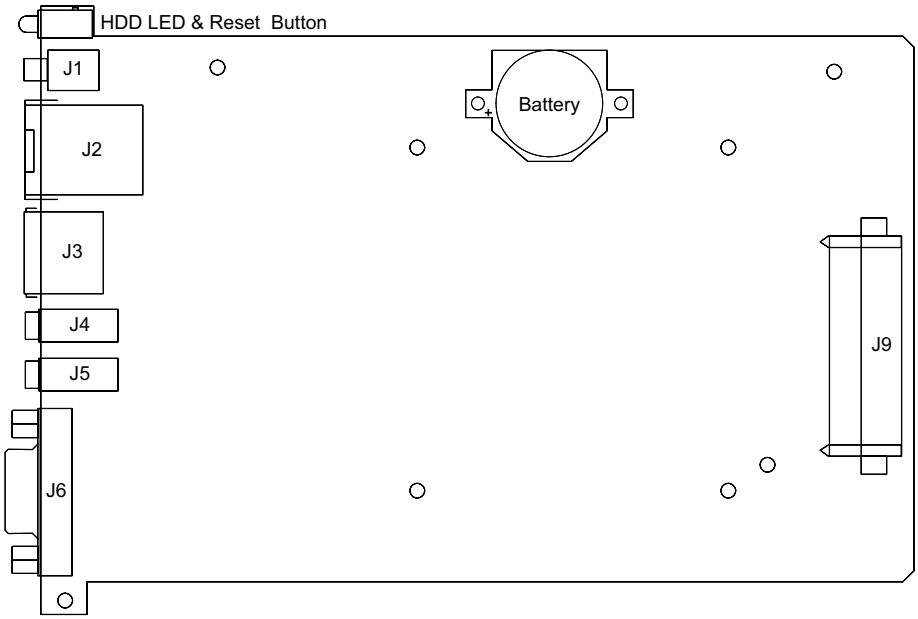
6.4 Front Panel of the CP3010-SA with CP3010-HDD Module

Figure 10: Front Panel of the 8 HP CP3010-SA with CP3010-HDD Module



6.5 CP3010-HDD Module Board Layout

Figure 11: CP3010-HDD Module Board Layout (Top View)



6.6 Module Interfaces (Front Panel and Onboard)

6.6.1 CAN Interface

The CP3010-HDD provides a standard CAN interface implemented as one standard, 9-pin D-Sub connector, J6.

6.6.2 Serial Port

The serial port is implemented as an 8-pin RJ-45 connector, J3.

Figure 12: Serial Port Connector J3

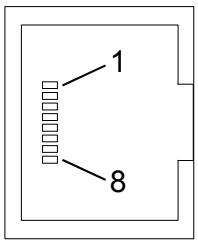


Table 39: Serial Port Connector J3 Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	RTS	Request to send	O
2	DTR	Data terminal ready	O
3	TXD	Transmit data	O
4	GND	Signal ground	--
5	GND	Signal ground	--
6	RXD	Receive data	I
7	DSR	Data send request	I
8	CTS	Clear to send	I

6.6.3 Gigabit Ethernet Interface

The CP3010-HDD provides a standard Gigabit Ethernet interface implemented as one standard, RJ-45 connector, J2.

6.6.4 USB Interface

The CP3010-HDD provides one standard, type A, USB 2.0 connector, J1.

6.6.5 Audio Interfaces

The CP3010-HDD module provides two audio interfaces, Line-In and Line-Out, implemented as two standard 3.5 mm audio stereo jacks on the front panel J4 (Line-In) and J5 (Line-Out).

The audio interfaces are provided with a HD audio codec chip (92HD73C1), which is connected directly to the HDA port of the SOC.

6.6.6 SATA Interface

The CP3010-HDD extension module provides a standard SATA connector, J9, for connecting a 2.5” SATA HDD/SSD.

7 CP-RIO3-04 Rear Transition Module

7.1 Overview

The CP3010-SA provides optional rear I/O connectivity for peripherals. Some standard PC interfaces are implemented and assigned to the front panel and to the rear I/O connector J2 on the CP3010-SA. When the CP-RIO3-04 rear transition module is used, some signals of main board/front panel connectors are routed to the module interface.

To support the rear I/O feature, a 3U CompactPCI backplane with rear I/O support is required. The CP-RIO3-04 rear transition module provides the following interfaces.

- CompactPCI rear I/O
- Two USB 2.0 ports
- Two Gigabit Ethernet ports without LED signals
- Two COM ports
- One VGA analog port
- Two SATA ports
- Power supply management

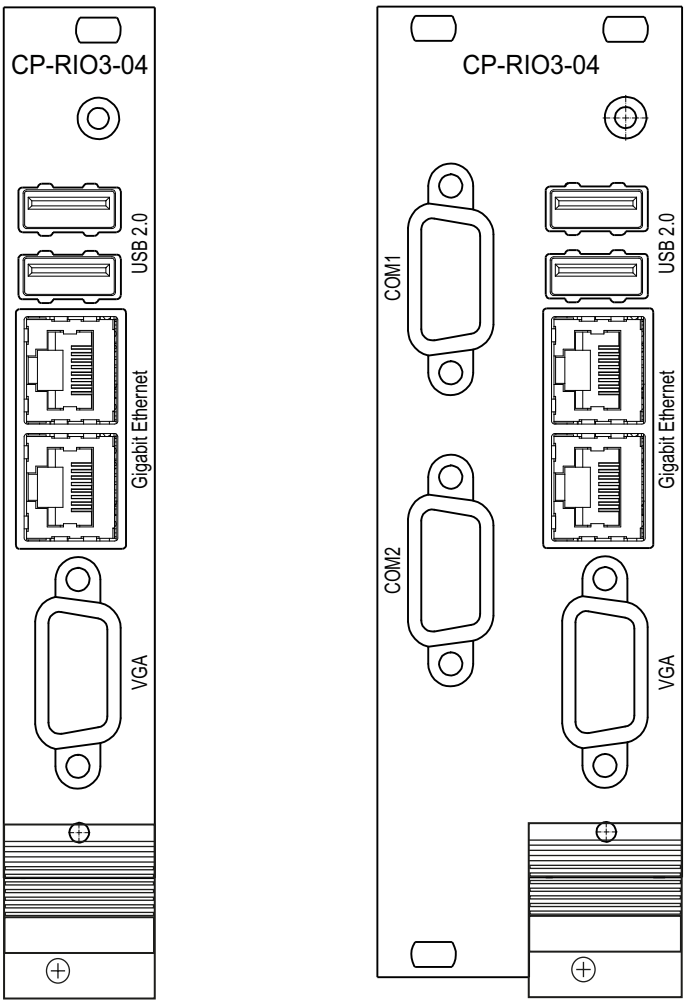
7.2 Technical Specifications

Table 40: CP-RIO3-04 Rear Transition Module Specifications

FEATURES		SPECIFICATIONS
External Interfaces	USB 2.0	Two USB 2.0 type A connectors, J11 and J12
	VGA	One VGA interface implemented as a 15-pin, D-Sub connector, J7
	Ethernet	Two Gigabit Ethernet interfaces implemented as a dual RJ-45 connector without LEDs, J10A/B
	Serial	Two onboard RS-232 serial ports with full modem support COMA (COM1) and COMB (COM2) implemented as: » 10-pin onboard connectors J2 (COMA) and J3 (COMB) on the 4 HP version » 9-pin, D-Sub connectors, J2a (COMA) and J3a (COMB) on the 8HP version
Internal Interfaces	CompactPCI	CompactPCI connector, rJ2, for rear I/O backplane connection
	SATA	Two SATA interfaces implemented as two 7-pin, L-form standard SATA connectors
	Serial	Two COM ports (COMA and COMB) implemented as two 10-pin, 2.54 mm onboard connectors with full modem support, J2 (COMB) and J3 (COMA) On the 8HP version, the serial ports are routed to the front panel and implemented as two 9-pin, D-Sub connectors, J2a (COM1) and J3a (COM2).
	Peripheral Control	One 10-pin, 2.54 mm onboard connector for power supply management, J13
General	Temperature Range	Operational: 0°C to +60°C Storage: -55°C to +85°C
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	100 mm x 80 mm
	Board Weight	4 HP: 120 grams 8HP: 150 grams

7.3 CP-RIO3-04 Front Panels

Figure 13: CP-RIO3-04 4HP and 8HP Front Panels



7.4 CP-RIO3-04 Rear Transition Module Layout

Figure 14: 4HP CP-RIO3-04 Rear Transition Module Layout

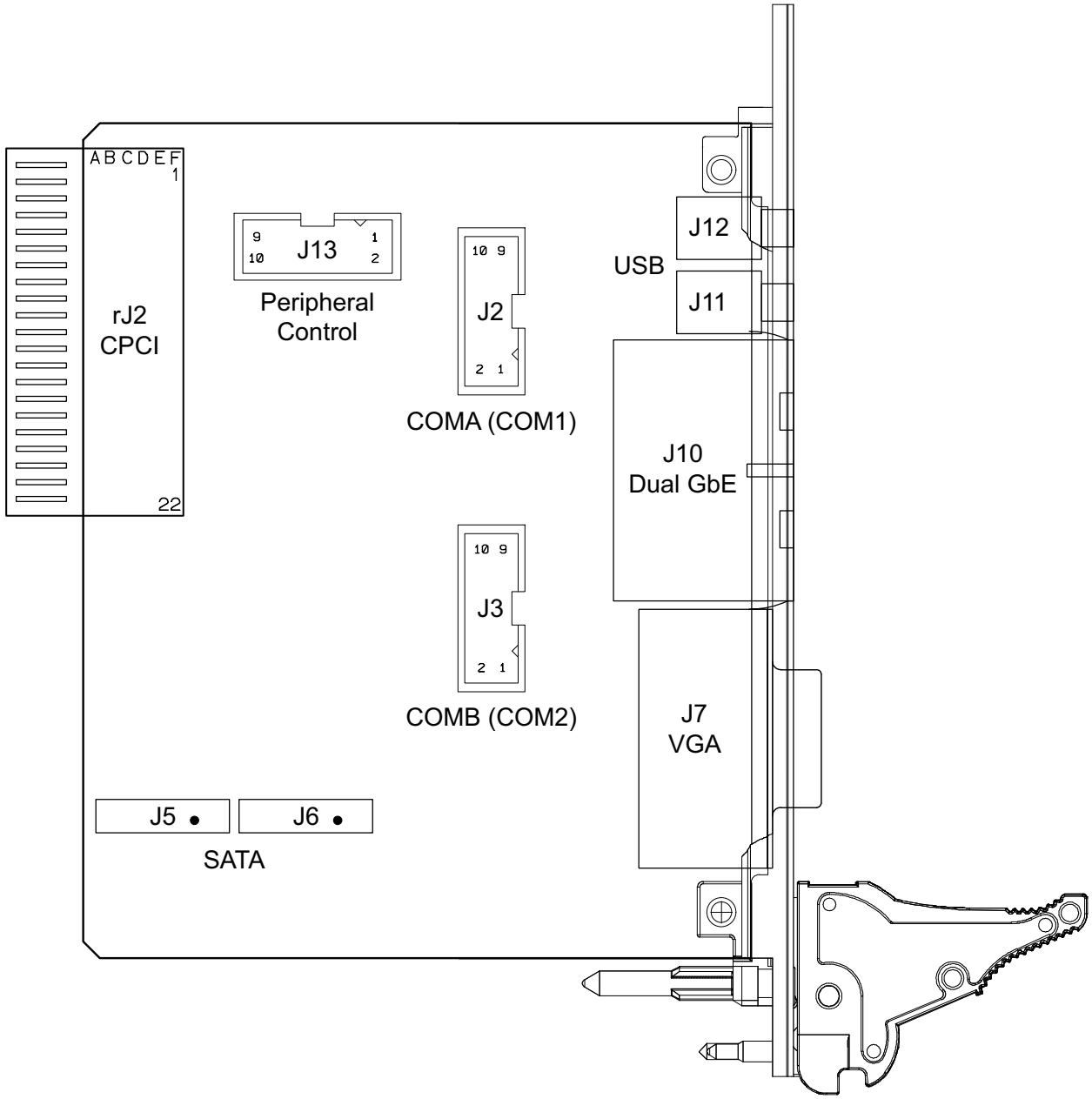
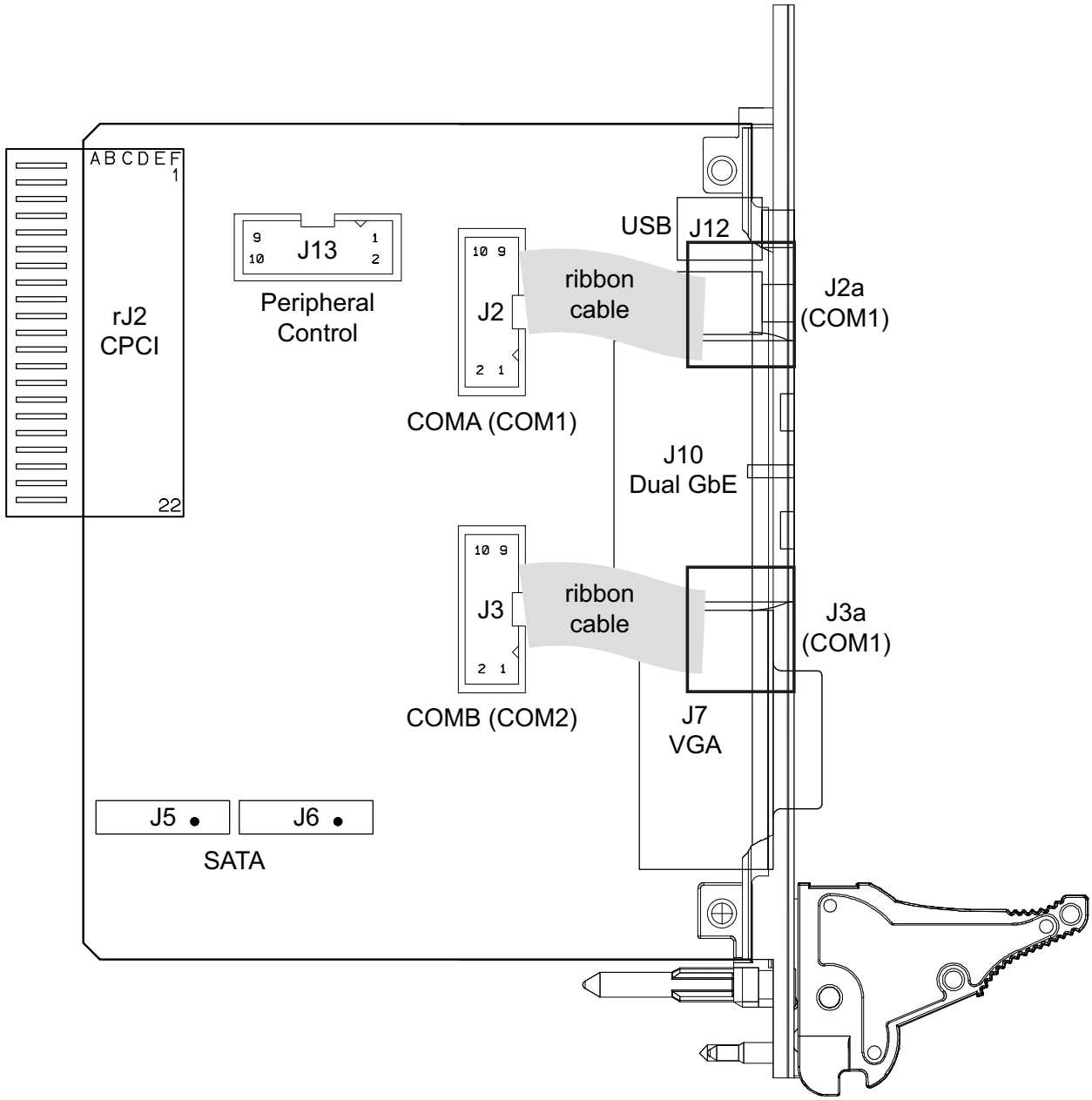


Figure 15: 8HP CP-RIO3-04 Rear Transition Module Layout



7.5 Module Interfaces

7.5.1 USB Interfaces

The CP-RIO3-04 rear transition module provides two standard, type A, USB 2.0 connectors, J11 and J12, on the front panel.

7.5.2 VGA Interface

The CP-RIO3-04 provides one standard VGA interface for connection to a monitor. The VGA interface is implemented as a standard VGA connector, J7. on the front panel.

7.5.3 Gigabit Ethernet Interface

The CP-RIO3-04 provides two Gigabit Ethernet interfaces realized as RJ-45 connectors without LEDs. The interface provides automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

7.5.4 COM Interface

The CP-RIO3-04 rear transition module provides two identical COM ports for connection to RS-232 devices. On the 8 HP version, the onboard 10-pin serial connectors J2 and J3 are routed to the 9-pin D-Sub COM connectors J2a and J3a located on the front panel. On the 4 HP version, the COM signals are available only on the onboard 10-pin serial port connectors J2 and J3.

The following table provides pinout information for the onboard serial port connectors J2 and J3. Refer to the module layout for connector and pin locations.

Table 41: Serial Port Connectors J2 (COMB) and J3 (COMA) Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	DCD	Data carrier detect	I
2	DSR	Data send request	I
3	RXD	Receive data	I
4	RTS	Request to send	O
5	TXD	Transmit data	O
6	CTS	Clear to send	I
7	DTR	Data terminal ready	O
8	RI	Ring indicator	I
9	GND	Signal ground	--
10	NC	Not connected	--

7.5.5 Peripheral Control Interface

A power supply with power management can be connected to the CP-RIO3-04 rear transition module via the peripheral control connector J13.

The following table provides pinout information for the peripheral control connector J13. Refer to the module layout for connector and pin locations.

Table 42: Peripheral Control Connector J13 Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	GND	Signal ground	--
2	PWR_5VSTDBY	+5V standby power (optional)	I
3	RSV	Reserved	--
4	VCC5V	Power +5V	O
5	RSV	Reserved	--
6	VCC3V3	Power +3.3V	O
7	PWR_SLPS3#	Power supply sleep mode	O
8	GND	Signal ground	--
9	PWR_BTN#	Wake-up / sleep input	I
10	GND	Signal ground	--

7.5.6 SATA Interfaces

The onboard SATA connectors J5 and J6 allow the connection of standard HDDs/SSDs and other SATA devices to the CP-RIO3-04 rear transition module.

7.5.7 Rear I/O Interface on CompactPCI Connector rJ2

The CP-RIO3-04 rear transition module conducts a wide range of I/O signals through the rear I/O connector rJ2.

Note: To support the rear I/O feature, a 3U CompactPCI backplane with rear I/O support is required. Do not plug a rear I/O configured board in a backplane without rear I/O support. Failure to comply with the above will result in damage to your board.

Figure 16: Rear I/O CompactPCI Connector rJ2

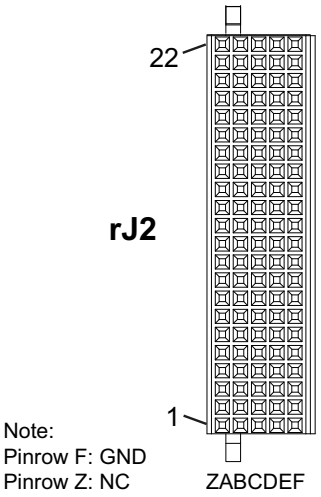


Table 43: Rear I/O CompactPCI Connector rJ2 Pinout

PIN	Z	A	B	C	D	E	F
22	NC	NC	NC	NC	NC	NC	GND
21	NC	NC	GND	USBA+/bi	USBB+/bi	USBA_PWR_5V/ in	GND
20	NC	NC	GND	USBA-/bi	USBB-/bi	USBB_PWR_5V/ in	GND
19	NC	GND	GND	PWR_BTN#/out	PWR_SLPS3#/in	RIO_3.3V/in	GND
18	NC	COMA_RXD/out	COMA_DCD#/out	COMA_DTR#/in	COMB_CTS# /out	COMA_CTS#/out	GND
17	NC	COMA_TXD/in	COMB_RXD/out	NC	NC	NC	GND
16	NC	COMA_DSR#/out	COMA_RTS#/in	NC	RSV	COMA_RI#/out	GND
15	NC	PWR_5VSTDBY/ out	RSV	NC	NC	NC	GND
14	NC	IPA_DA+/bi	IPA_DA-/bi	COMB_RTS#/in	IPA_DC+/bi	IPA_DC-/bi	GND
13	NC	IPA_DB+/bi	IPA_DB-/bi	COMB_RI#/out	IPA_DD+/bi	IPA_DD-/bi	GND
12	NC	IPB_DA+/bi	IPB_DA-/bi	RIO_1V9/in	IPB_DC+/bi	IPB_DC-/bi	GND
11	NC	IPB_DB+/bi	IPB_DB-/bi	COMB_DCD#/out	IPB_DD+/bi	IPB_DD-/bi	GND
10	NC	GND	COMB_TXD/in	VGA_RED/in	COMB_DTR#/in	GND	GND
9	NC	SATAATX+/in	GND	VGA_HSYNC/in	GND	SATABTX+/in	GND
8	NC	SATAATX-/in	GND	VGA_BLUE/in	GND	SATABTX-/in	GND
7	NC	GND	COMB_DSR#/out	VGA_DDC_DATA/bi	RSV	GND	GND
6	NC	SATAARX+/out	GND	VGA_GREEN/in	GND	SATABRX+/out	GND
5	NC	SATAARX-/out	GND	VGA_VSYNC/in	GND	SATABRX-/out	GND
4	NC	NC	RIO_5V/in	VGA_DDC_CLK/in	GPIO_CFG0/out	GND	GND
3	NC	NC	GND	NC	NC	NC	GND
2	NC	NC	NC	NC	NC	NC	GND
1	NC	NC	NC	NC	NC	NC	GND

Note: The RIO_XXX signals are power supply **INPUTS** to supply the rear I/O module with power. These pins **MUST NOT** be connected to any other power source, either within the backplane itself or within a rear I/O module. Failure to comply with the above will result in damage to your board.

Table 44: Rear I/O Signal Description

SIGNAL	DESCRIPTION
COMAx	COMA port LVTTL (3.3V)
COMBx	COMB port LVTTL (3.3V)
GPIO_CFG0	GPIO or COMB configuration
IPx	Gigabit Ethernet copper port
SATAx	SATA port
USBx	USB interface and power
VGAx	VGA signal
RIOx/VI/O	Power supply signal
PWRx	Power management signal
RSV	Reserved
GND	Ground signal
NC	Not connected

8 Installation

This chapter is oriented towards an application environment. Some aspects may, however, be applicable to a development environment.

8.1 Safety

To ensure personnel safety and correct operation of this product, the following safety precautions must be observed:

- All operations involving the CP3010-SA require that personnel be familiar with system equipment, safety requirements and the CP3010-SA.
- This product contains electrostatically sensitive components which can be seriously damaged by electrical static discharge (ESD). Therefore, proper handling must be ensured at all times.
- Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.
- Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.
- Do not touch components, connector-pins or traces.

Kontron assumes no liability for any damage resulting from failure to comply with these requirements.

8.2 General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

8.3 Board Installation

The CP3010-SA is designed for use either as a CompactPCI system controller or as an autonomous CPU board in a CompactPCI peripheral slot.

When installed in the system slot, the CP3010-SA provides all required functions for supporting the hot swapping of peripheral boards which are capable of being hot swapped. In this configuration the CP3010-SA itself is not hot-swappable.

When installed in a CompactPCI peripheral slot, the CP3010-SA operates autonomously, meaning that it only draws power from the CompactPCI backplane. There is no interfacing with the CompactPCI bus, clocks or other control signals. In this configuration, the CP3010-SA supports hot plugging. This simply means that the board can be installed or removed from the system while under power.

Note: Always ensure that all functions in progress are properly terminated or put into a safe state prior to hot plugging the CP3010-SA.
Failure to comply with the above may result in improper operation or damage to other system components, e.g. operating system failure, data loss, uncontrolled processing, etc.

Note: In order to use the hot plug function of the CP3010-SA, a hot swap-capable backplane is required.

8.3.1 Standard Board Insertion

Prior to following the steps below, ensure that the safety requirements are met.

To insert the CP3010-SA in a system proceed as follows:

1. Ensure that no power is applied to the system before proceeding.
2. Insert the board into the slot designated until it makes contact with the backplane connectors.
3. Using the ejector handle, engage the board with the backplane. When the ejector handle is closed, the board is engaged.
4. Fasten the front panel retaining screws.
5. Connect all external interfacing cables to the board as required.

8.3.2 Standard Board Removal

Prior to following the steps below, ensure that the safety requirements are met. When removing a board from the system, particular attention must be paid to the components which may be hot, such as heat sink, etc.

To remove the CP3010-SA from a system proceed as follows:

1. Ensure that no power is applied to the system before proceeding.
2. Disconnect any interfacing cables that may be connected to the board.
3. Unscrew the front panel retaining screws.
4. Unlock the ejector handle.
5. Disengage the board from the backplane by pressing the handle as required and remove the board from the system.

8.4 CFast Card Installation

The CP3010-SA provides optional support for a CFast card. For the location of the CFast card socket on the, refer to Figure 3.

To preclude damage or data loss when removing the CFast Card, ensure that the operating system has been informed of the pending removal and that the OS has indicated that it is safe to proceed.

8.5 Rear Transition Module Installation

The CP-RIO3-04 rear transition module does not support hot swapping. Therefore, the system must have power removed to install or remove the CP-RIO3-04 rear transition module. Before extracting the CP-RIO3-04 rear transition module, ensure that all connected cables are disconnected.

8.6 Battery Replacement

The CP3010-SA RTC may be backed up using a single 3.0 V “coin cell” lithium battery from one of two possible points of installation:

- onboard
- on the extension module

Only one battery may be installed at a time. Refer to Table 1 for battery requirements.

9 uEFI BIOS

9.1 Starting the uEFI BIOS Setup Program

The CP3010-SA is provided with a Kontron-customized, pre-installed and configured version of SecureCore Tiano™ (referred to as uEFI BIOS in this manual), Phoenix BIOS firmware based on the Unified Extensible Firmware Interface (uEFI) specification and the Intel® Platform Innovation Framework for EFI. This uEFI BIOS provides a variety of new and enhanced functions specifically tailored to the hardware features of the CP3010-SA.

The uEFI BIOS comes with a Setup program which provides quick and easy access to the individual function settings for control or modification of the uEFI BIOS configuration. The Setup program allows the accessing of various menus which provide functions or access to sub-menus with more specific functions of their own.

To start the uEFI BIOS Setup program, follow the steps below:

1. Power on the board.
2. Wait until the first characters appear on the screen (POST messages or splash screen).
3. Press the <F2> key.
4. If the uEFI BIOS is password-protected, a request for password will appear.

   Enter either the User Password or the Supervisor Password (see Security menu), press <RETURN>, and proceed with step 5.
5. A Setup menu will appear.

To launch the uEFI BIOS Boot Menu, follow the steps below:

1. Power on the board.
2. Wait until the first characters appear on the screen (POST messages or splash screen).
3. Press the <F5> key.
4. The uEFI BIOS Boot Menu will appear.

The CP3010-SA uEFI BIOS Setup program uses a hot key-based navigation system. A hot key legend bar is located on the bottom of the Setup screens. The following table provides information concerning the usage of these hot keys.

Table 45: Navigation

HOT KEY	DESCRIPTION
<F1>	The <F1> key is used to invoke the General Help window.
<F5> or <->	The <F5> key or the <Minus> key is used to select the next lower value within a field.
<F6> or <+>	The <F6> key or the <Plus> key is used to select the next higher value within a field.
<F9>	The <F9> key is used to load the standard default values.
<F10>	The <F10> key is used to save the current settings and exit the uEFI BIOS Setup.
<→> <←>	The <Left/Right> arrows are used to select major Setup menus on the menu bar. For example: Main screen, Advanced screen, Security screen, etc.
<↑> <↓>	The <Up/Down> arrows are used to select fields in current menu, for example, a Setup function or a sub-screen.
<ESC>	The <ESC> key is used to exit a major Setup menu and enter the Exit Setup menu. Pressing the <ESC> key in a sub-menu causes the next higher menu level to be displayed.
<RETURN>	The <RETURN> key is used to execute a command or select a submenu.

9.2 Setup Menus

The Setup utility features four menus listed in the selection bar at the top of the screen:

- Main
- Advanced
- Security
- Boot
- Exit

The Setup menus are selected via the left and right arrow keys. The currently active menu and the currently active uEFI BIOS Setup item are highlighted in white. Each Setup menu provides two main frames. The left frame displays all available functions. Functions that can be configured are displayed in blue. Functions displayed in gray provide information about the status or the operational configuration. The right frame displays an Item Specific Help window providing an explanation of the respective function.

9.2.1 Main Setup Menu

Upon entering the uEFI BIOS Setup program, the Main Setup menu is displayed. This screen lists the Main Setup menu sub-screens and provides basic system information as well as functions for setting the system time and date.

Table 46: Main Setup Menu Sub-Screens and Functions

SUB-SCREEN	FUNCTION	DESCRIPTION
System Information	BIOS Version, Build Time, etc.	Read-only field. Displays information about the system BIOS, processor, memory, etc.
Boot Features	CSM Support	Enables/Disables Compatibility Support Module
	Quick Boot	Enables/Disables time-optimized POST, causing certain preconfigured OEM optimizations to be made when the system boots.
	BIOS Level USB	Enables/Disables backward compatibility for legacy BIOS services.
	Console Redirection	Enables/Disables console redirection over serial port.
	Com Port	Selects the specific COM port The COM1 port corresponds to the COMA port. The COM0 port corresponds to the COMB port.
	Terminal Type	Selects the terminal type to be emulated.
	Baudrate	Selects the baud rate of the serial port.
	Flow Control	Specifies the type of flow control to be used for the serial port.
	Continue C.R. after POST	Enables/Disables console redirection after the operating system has loaded.
	UEFI Boot	Enables/Disables uEFI Boot.
	Legacy Boot	Enables/Disables Legacy Boot.
	Boot Priority	Selects the priority of boot option between uEFI Boot and Legacy Boot.

9.2.2 Advanced Setup Menu

The Advanced Setup menu provides sub-screens and functions for advanced configuration.

Note: Setting items on this screen to incorrect values may cause the system to malfunction.

Table 47: Advanced Setup Menu Sub-Screens and Functions

SUB-SCREEN	FUNCTION	DESCRIPTION
Uncore Configuration	GOP Configuration	
	GOP Driver	Enables/Disables GOP Driver. If enabled, the GOP Driver will unload VBIOS. If disabled, GOP Driver will load VBIOS.
South Cluster Configuration	USB Configuration	Specifies the USB Configuration settings.
	EHCI Controller	Controls the USB EHCI (USB 2.0) functions. One EHCI controller must always be enabled.
	xHCI Mode	Specifies the mode of operation of the xHCI controller.
	XHCI Link Power Management	Enables/Disables the XHCI Link Power Management.
Security Configuration	TXE Configuration	
	TXE	Enables /Disables Trusted Execution Engine (TXE).
	TXE HMRFPO	Enables/Disables TXE HMRFPO. If "Disabled" is selected, the TXE firmware is temporarily disabled for the 1st boot cycle. The function is used for cloning via the **kFlash** uEFI Shell command.
	TXE Firmware Update	Enables/Disables TXE Firmware Update.
	TXE EOP Message	Enables/Disables TXE EOP Message. If enabled, it sends the EOP Message before entering the OS.
	TXE Unconfiguration Perform	Revert TXE settings to factory defaults.
OS Selection	--	Selects the operating system (Windows or Linux).

9.2.3 Security Setup Menu

The Security Setup menu provides information about the passwords and functions for specifying the security settings. The passwords are case-sensitive. The CP3010-SA provides no factory-set passwords.

Table 48: Security Setup Menu Functions

FUNCTION	DESCRIPTION
Supervisor Password is:	Read-only field.
User Password is:	Read-only field.
Set Supervisor Password	Sets or clears the Supervisor Password.
Supervisor Hint String	Press "Enter" to specify a hint string for the Supervisor Password.
Set User Password	Sets or clears the User Password.
User Hint String	Press "Enter" to specify a hint string for the User Password.
Min. password length	Specifies the minimum password length.
Authenticate User on Boot	Enables the user authentication prompt on the boot.
HDD Password Select	Specifies whether to enable User-only support for HDD or User and Master support.
HDD00 Password State	Read-only field.
Set HDD00 User Password	Specifies and confirms the HDD User Password.
Set HDD00 Master Password	Specifies and confirms the HDD Master Password.
TPM Support	Enables/Disables TPM support.

Note: If there is already a password installed, the system asks for this first. To clear a password, simply enter nothing and acknowledge by pressing <RETURN>. To set a password, enter it twice and acknowledge by pressing <RETURN>.

Table 49: TPM Configuration Sub-Screen

FUNCTION	DESCRIPTION
Current TPM State	Read-only field.
TPM Action	Enacts TPM Action. Note: Most TPM actions require TPM to be Enabled to take effect.
Omit Boot Measurements	Enabling this option causes the system to omit recording boot device attempts in PCR[4].

9.2.3.1 Remember the Password

It is highly recommended to keep a record of all passwords in a safe place. Forgotten passwords may lead to being completely locked out of the system.

If the system cannot be booted because neither the User Password nor the Supervisor Password are known, refer to the Chapter 3.1, DIP Switch Configuration, for information about clearing the uEFI BIOS settings, or contact Kontron for further assistance.

Note: The HDD security passwords cannot be cleared using the above method.

9.2.4 Boot Setup Menu

The Boot Setup menu lists the boot device priority order, which is dynamically generated.

Table 50: Boot Priority Order

FUNCTION		DESCRIPTION
Boot Priority Order	1. Internal Shell	Keys used to view or configure devices: <↑> and <↓> arrows select a device. <+> and <-> move the device up or down. <Shift + 1> enables or disables a device. <Del> deletes an unprotected device.
	2. USB FDD:	
	3. USB CD:	
	4. ATAPI CD:	
	5. USB HDD:	
	6. ATA HDD0:	
	7. ATA HDD1:	
	13. PCI LAN:	

9.2.5 Exit Setup Menu

The Exit Setup menu provides functions for handling changes made to the uEFI BIOS settings and the exiting of the Setup program.

Table 51: Exit Setup Menu Functions

FUNCTION	DESCRIPTION
Exit Saving Changes	Equal to F10, save all changes of all menus, then exit the uEFI BIOS Setup. Finally, resets the system automatically.
Exit Discarding Changes	Never save changes, then exit the uEFI BIOS Setup.
Load Setup Defaults	Equal to F9. Load standard default values.
Discard Changes	Load the original value of this boot time, not the default Setup value.
Save Changes	Save all changes of all menus, but do not reset system.

9.3 The uEFI Shell

The Kontron uEFI BIOS features a built-in and enhanced version of the uEFI Shell. For a detailed description of the available standard shell scripting refer to the EFI Shell User's Guide. For a detailed description of the available standard shell commands, refer to the EFI Shell Command Manual. Both documents can be downloaded from the EFI and Framework Open Source Community homepage (http://sourceforge.net/projects/efi-shell/files/documents/).

Please note that not all shell commands described in the EFI Shell Command Manual are provided by the Kontron uEFI BIOS.

9.3.1 Introduction, Basic Operation

The uEFI Shell forms an entry into the uEFI boot order and is the first boot option by default.

9.3.1.1 Entering the uEFI Shell

To enter the uEFI Shell, follow the steps below:

1. Power on the board.
2. Ignore the message: "Press the <F2> key".
3. Press the ESC key within 5 seconds after a message such as the one below appears:

```
EFI Shell version 2.31 [4660.22136]
Current running mode 1.1.2
Device mapping table
blk0      :Removable HardDisk - Alias hd33b0b0b fs0
           Acpi(PNP0A03,0)/Pci(1D|7)/Usb(1, 0)/Usb(1, 0)/HD(Part1,Sig17731773)
...
Press the ESC key within 5 seconds to skip startup.nsh, and any other key to
continue.
```

The output produced by the device mapping table can vary depending on the board's configuration.

If the ESC key is pressed before the 5-second timeout has elapsed, the shell prompt is shown:

```
Shell>
```

9.3.1.2 Exiting the uEFI Shell

To exit the uEFI Shell, follow one of the steps below:

1. Invoke the **exit** uEFI Shell command to select the boot device in the boot menu for the OS to boot from.
2. Reset the board using the **reset** uEFI Shell command.

9.3.2 Kontron-Specific uEFI Shell Commands

The Kontron uEFI implementation provides the following additional commands related to the specific HW features of the Kontron system.

Table 52: Kontron-Specific uEFI Shell Commands

COMMAND	DESCRIPTION
kBoardConfig	Configures non-volatile board settings, such as: » Pxe » PrimaryDisplay » VGA » COMA » Usb » GbeA » GbeB » SataMode » SataSpeed » Sata0Hotplug » Sata1Hotplug » IntelVT » SpeedStep » CpuTurbo » CState » WrProtSystem » WrProtSata » AutoUpdate If AutoUpdate is enabled, an automatic update procedure from the connected mass storage device is initiated after a reset. The update status is indicated in the log file located in the directory where the firmware images are stored. » Shell Timeout **Note:** The parameters of the kBoardConfig command are not case-sensitive.
kBoardInfo	Shows a summary of board-specific data and displays/checks various parameters such as the current uEFI BIOS revision, etc.
kBootScript	Manages the flash-stored startup script If the shell is launched by the boot process, it executes a shell script stored in the flash. If the shell script terminates, the shell will continue the boot process. However, the shell script can also contain any other boot command.
kFlash	Programs and verifies the SPI boot flashes holding the uEFI BIOS code uEFI BIOS binary files must be available from connected mass storage devices, such as USB flash drive or harddisk.
kJtag	Programs an onboard device via the JTAG interface.
kNvram	Manages the NVRAM to restore the system's default settings Since all uEFI settings are stored inside the NVRAM, the default settings are loaded after invoking this command.

Table 52: Kontron-Specific uEFI Shell Commands

COMMAND	DESCRIPTION
kPassword	Controls uEFI Setup and Shell passwords This command is used to determine the status of both passwords (set or not set) and to set or clear the uEFI Shell and Setup passwords. Both user and superuser (Supervisor) passwords can be controlled with this command. Call without options to get current password status. Entering an empty password clears the password.
kRamdisk	Creates and manages RAMdisks This command is used to perform file operations when no real filesystem is connected to the system.
kReset	Controls the board's reset behavior This command controls if the board shall react on a CompactPCI backplane reset if it is used in a peripheral slot. It has no effect if the board is installed in the CompactPCI system slot. The parameter of this command is volatile and set to off at the next start.
kUpdate	Controls the Kontron common update tool When using the **kUpdate** command, the structure of the ZIP archive must not be altered. **kUpdate** automatically starts the update procedure via **kUpdate -u.** If a certain image is intended to be used, enter **kUpdate -s** to select the respective image.
kWatchdog	Configures the Kontron onboard Watchdog This command is used to enable the Kontron onboard Watchdog with reset target before OS boot. This can be used to detect if the OS fails to boot and react by reset.

The uEFI Shell commands are not case-sensitive. Each uEFI Shell command is provided with a detailed online help that can be invoked by entering "<cmd> <space> <-?>" in the command line. To display the uEFI Shell command list, enter <help> or <?> in the command line.

9.4 uEFI Shell Scripting

9.4.1 Startup Scripting

If the ESC key is not pressed and the timeout is run out, the uEFI Shell tries to execute some startup scripts automatically. It searches for scripts and executes them in the following order:

1. Kontron flash-stored startup script
2. If there is no Kontron flash-stored startup script present, the uEFI-specified **`startup.nsh`** script is used. This script must be located on the root of any of the attached FAT-formatted disk drive.
3. If none of the startup scripts is present or the startup script terminates, the default boot order is continued.

9.4.2 Create a Startup Script

Startup scripts can be created using the uEFI Shell built-in editor **edit** or under any OS with a plain text editor of your choice. To create a startup shell script, simply save the script on the root of any FAT-for-

matted drive attached to the system. To copy the startup script to the flash, use the **kBootScript** uEFI Shell command.

In case there is no mass storage device attached, the startup script can be generated in a RAM disk and stored in the SPI boot flash using the **kRamdisk** uEFI Shell command.

9.4.3 Examples of Startup Scripts

9.4.3.1 Execute Shell Script on Other Harddrive

This example (`startup.nsh`) executes the shell script named `bootme.nsh` located in the root of the first detected disc drive (`fs0`).

```
fs0:
bootme.nsh
```

9.4.3.2 Enable Watchdog

The uEFI Shell provides an environment variable used to control the execution flow. The following sample start-up script shows the uEFI Shell environment variable `wdt_enable` used to control the Watchdog.

```
echo -off
echo "Executing sample startup.nsh..."
if %wdt_enable% == "on" then
   kwatchdog -t 15
   echo "Watchdog enabled"
endif
```

To create a uEFI Shell environment variable, use the **set** uEFI Shell command as shown below:

```
Shell> set wdt_enable on
Shell> set
   wdt_enable : on
Shell> reset
```

9.4.3.3 Handling the Startup Script in the SPI Boot Flash

In case there is no mass storage device attached, the startup script can be generated in a RAM disk and stored in the SPI boot flash using the following instructions:

1. Press <ESC> during power-up to log into the uEFI Shell.

2. Create a RAM disk and set the proper working directory as shown below:

```
Shell> kramdisk -s 3 -c -m myramdisk
Shell> myramdisk:
```

3. Enter the sample start-up script mentioned above in this section using the **edit** uEFI Shell command.

```
myramdisk:\> edit boot.nsh
```

4. Save the start-up script to the SPI boot flash using the **kBootScript** uEFI Shell command.

```
myramdisk:\> kbootscript -p boot.nsh
```

5. Reset the board to execute the newly installed script using the **reset** uEFI Shell command.

```
myramdisk:\> reset
```

6. If a script is already installed, it can be edited using the following **kBootScript** uEFI Shell commands:

```
myramdisk:\> kbootscript -g boot.nsh
myramdisk:\> edit boot.nsh
```

9.5 Firmware Update

Firmware updates are typically delivered as a ZIP archive containing only the firmware images. The content of the archive with the directory structure must be copied on a data storage device with FAT partition. If the command **kBoardConfig AutoUpdate** has been enabled, the images are automatically detected during boot-up and an update of the uEFI BIOS is carried out.

9.5.1 Updating the uEFI BIOS

9.5.1.1 uEFI BIOS Fail-Over Mechanism

The CP3010-SA has two SPI boot flashes programmed with the uEFI BIOS, a standard SPI boot flash and a recovery SPI boot flash. The basic idea behind that is to always have at least one working uEFI BIOS flash available regardless if there have been any flashing errors or not.

9.5.1.2 Updating Procedure

The standard SPI boot flash can be updated with the latest uEFI BIOS from the ZIP archive using the **kUpdate -u** or the **kFlash -p** uEFI Shell command. When using the **kUpdate** command, the directory structure of ZIP archive must not be altered. The update status is indicated in the log file located in the directory where the firmware images are stored.

9.5.1.3 uEFI BIOS Recovery

In case of the standard SPI boot flash being corrupted and therefore the board not starting up, the board can be booted from the recovery SPI boot flash if the DIP switch SW1, switch 2 is set to ON. For further information, refer to the Chapter 3.1, DIP Switch Configuration.

Note: The uEFI BIOS code and settings are stored in the SPI boot flashes. Changes made to the uEFI BIOS settings are available only in the currently selected SPI boot flash. Thus, switching over to the other SPI boot flash may result in operation with different uEFI BIOS code and settings.

9.5.1.4 Determining the Active Flash

Sometimes it may be necessary to check which flash is active. On the uEFI BIOS, this information is available via the **kBoardInfo** uEFI Shell command.

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